DATA I/O

DTI 950-0099-1

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CALIBRATION CERTIFICATION

CUSTOMER. . .MCDONELL DOUGLAS

P.O. NO. . .57162838

MODEL. . . .950-0099-009

DESCRIPTION . .UNIPAK

SERIAL NO. . .AA04462

CAL DATE . . .02-14-85

NEXT CAL DATE .08-14-85

THIS INSTRUMENT WAS CALIBRATED UNDER DATA I/O WORKMANSHIP STANDARDS AND QUALITY ASSURANCE PROGRAM. IT IS CERTIFIED THAT THIS SYSTEM MEETS ALL MANUFACTURING SPECIFICATIONS. THE STANDARDS USED HAVE BEEN COMPAIRED AT PLANNED INTERVALS WITH THE NATIONAL STANDARDS EITHER DIRECTLY OR INDIRECTLY. THE SYSTEM IS DESIGNED TO ENSURE THAT ESTABLISHED SCHEDULES AND PROCEDURES ARE FOLLOWED TO MAINTAIN THE ACCURACY OF ALL MEASURING AND TEST STANDARDS USED BY DATA I/O IN THIS CALIBRATION.

TESTED AND APPROVED BY: D. Tefft 3604

904 15216

DTI 950-0099-1

UniPak ™

981-0003-001 REV A SEPT 84

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NOTE

This configuration of the UniPak™ varies from previous configurations in that it uses some hexadecimal family codes. Some decimal family numbers have been changed. While this configuration will work with any Data I/O Universal Programmer (see section 1.1), to use hexadecimal families it may be necessary to update your programmer. Refer to section 1.2 of this manual for maintenance compatibility requirements. Model 1730s cannot handle hexadecimal families at this time. Some of the new larger devices will require that the programmer RAM be expanded. Consult your nearest Data I/O representative for update availability.

Applies to: Engineering Part Number 950-0099-009
Text Part Number 090-0064-001

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008-1999	Motherboard
30-701-7997	Waveform Generator
30-702-0045	UniPak™ Memory
30-702-7995	Socket Assembly

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SYSTEM 19
Operator's Synopsis

STANDARDS COPY

004 1900 August 1980

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Notes on Handling Equipment

- To retain data in programmer RAM, Programming Paks and socket adapters may be exchanged with power ON.
- Do not switch power or exchange Programming Paks with a device in the socket
- Do not insert or remove a device while the START light is ON.

Notes on Key Operations

- To clear a miskeyed value, press the function key again
- To reset the programmer, press KEYBD.
- *Optional keystrokes are in italics*
- Refer to the System 19 manual and the programming electronics manual for complete information on all operations

Load, Program and Verify

- Press LOAD, PROG or VER
- *Key in the Family Code (XX) with UniPak only*
- *Key in the Pinout Code (YY) with UniPak only*
- Insert device
- Press START
- When the COMPLETE light comes ON, observe displayed sum-check

UNIPAK

Keyboard Data Entry and Editing

Change
- Press KEYBD
- Key in address
- Press ENTER
- Key in data
- Press ENTER

New data replaces old data.

Insert
- Press KEYBD
- Key in address
- Press ENTER
- Press EDIT
- Key in data
- Press INSERT

Data at the displayed address and each higher address moves one location higher. Data that was at highest absolute RAM address is lost

Delete
- Press KEYBD
- Key in address
- Press ENTER
- Press EDIT
- Press DELETE

Data at selected address is lost. All data words at higher addresses move one address lower. Highest absolute RAM address clears to 0

Keyboard Data Entry and Editing

Change

- Press KEYBD
- Key in address
- Press ENTER
- Key in data
- Press ENTER

New data replaces old data.

Insert

- Press KEYBD
- Key in address
- Press ENTER
- Press EDIT
- Key in data
- Press INSERT

Data at the displayed address and each higher address moves one location higher. Data that was at highest absolute RAM address is lost.

Delete

- Press KEYBD
- Key in address
- Press ENTER
- Press EDIT
- Press DELETE

Data at selected address is lost. All data words at higher addresses move one address lower. Highest absolute RAM address clears to Ø.

Block Moves

Device-to-RAM and RAM-to-Device

- Press BLOCK LIMITS
- Key in L1 (Begin RAM Address)
- Press ENTER
- Key in L2 (number of bytes)
- Press ENTER
- Key in L3 (Begin Device Address)
- Press ENTER
- Press LOAD, PROG or VER
- Press START

RAM-to-RAM

- Press BLOCK LIMITS
- Key in L1 (RAM Source Address)
- Press ENTER
- Key in L2 (number of bytes)
- Press ENTER
- Key in desired L3 (RAM Destination Address)
- Press ENTER
- Press SELECT
- Key in A7
- Press START

Select Codes

Select Code Key Sequence

- Press SELECT
- Key in Select Code
- *Press ENTER*
- *Key in parameter value*
- Press START

RAM Data Manipulation Select Codes

A1	Swap nibbles
A2	Fill memory with variable
A3	Complement memory
A4	Clear RAM
A5	Split RAM data
A6	Shuffle RAM data
A7	RAM-RAM block move

I/O Operation Select Codes

DØ	Output (with Remote Control)
D1	Input via serial port
D2	Input (with instrument control)
D3	Input compare
D4	Input compare (with instrument control)
D5	Output
D6	Output (with instrument control)

I/O Format Select Codes

10	Binary
11	DEC Binary
01(05)*	ASCII-BNPF
02(06)*	ASCII-BHLF
03(07)*	ASCII-B1ØF
08(09)*	5 level BNPF
12(13)*	Spectrum
30(35)†	ASCII-Octal(Space)
31(36)†	ASCII-Octal(Percent)
32	ASCII-Octal(Apostrophe)

Gang Programming Module, 950-0074 or 950-0075

24	Verify error
31	Excessive current drain
32	Backwards device
34	Faulty Characterizer
35	Faulty chip select
36	Programming block too small
38	Illegal operation during calibration

UniPak, 950-0099; MOS Pak, 950-0076

30	No programming algorithm
31	Excessive current drain
32	Backwards device
35	Faulty chip select
37	Socketing error
38	Illegal operation during calibration
70	Faulty bit supply
71	Faulty CS supply
72	Faulty Vcc supply

Simple I/O

Input or Input Compare

First byte to address ∅

- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press START
- Observe displayed sum-check

First byte to Begin RAM Address

- Press BLOCK LIMITS
- Key in L1 (Begin RAM Address)
- Press ENTER
- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press START
- Observe displayed sum-check

First byte to address IA−AO (first input address minus Address Offset)

- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press ENTER
- Key in Address Offset value
- Press START
- Observe displayed sum-check

First byte to BR + IA−AO where BR is Begin RAM Address IA is first input address AO is Address Offset

- Press BLOCK LIMITS
- Key in L1 (Begin RAM Address)
- Press ENTER
- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press ENTER
- Key in Address Offset value
- Press START
- Observe displayed sum-check

Output

First byte from address ∅

- Press BLOCK LIMITS
- Press ENTER
- Key in L2 (number of bytes)
- Press ENTER
- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press START
- Observe displayed sum-check

First byte from Begin RAM Address

- Press BLOCK LIMITS
- Key in L1 (Begin RAM Address)
- Press ENTER
- Key in L2 (number of bytes)
- Press ENTER
- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press START
- Observe displayed sum-check

First byte from RAM address ∅, but addressed with an Address Offset

- Press BLOCK LIMITS
- Press ENTER
- Key in L2 (number of bytes)
- Press ENTER
- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press ENTER
- Key in Address Offset value
- Press START
- Observe displayed sum-check

First byte from Begin RAM Address, but addressed with an Address Offset

- Press BLOCK LIMITS
- Key in L1 (Begin RAM Address)
- Press ENTER
- Key in L2 (number of bytes)
- Press ENTER
- *Press SELECT*
- *Key in format Select Code*
- *Press ENTER*
- Press SELECT
- Key in operation Select Code
- Press ENTER
- Key in Address Offset value
- Press START
- Observe displayed sum-check

Computer Remote Control

Control Commands

RETURN	Execute a command
ESC	Abort a command
BREAK	Abort a binary transfer

Utility Commands

G	Display the software-configuration number
HHHH <	Define Begin RAM "HHHH"
HHHH ;	Define number of bytes "HHHH"
HHHH :	Define Begin Device "HHHH"
HH)	Select extended software option "HH"
H	No-operation command
F	Error-status inquiry
X	Programmer outputs up to 16 error codes stored in scratch-pad RAM
S	Sum-check command
Z	Return control to the programmer

Device Commands

T	Test for illegal bit in device
B	Make blank check of device
P	Program RAM data into device
V	Verify device with RAM
L	Load device data into RAM
FFPP @	Select Family and Pinout (UniPak)
[	Inquire Family and Pinout (UniPak)
R	Respond command

I/O Commands

D	Select odd parity
E	Select even parity
N	Select no parity
J	Set one stop bit
K	Set two stop bits
HH M	Select record size
HH U	Set nulls
HHHH W	Set Address Offset
FC A	Select translation format code
=	Disable 25 second timeout
I	Input data from computer to RAM
O	Output data from RAM to computer
C	Compare data in RAM with computer data
Y	Parity-error inquiry

Editing Commands

Q	Swap nibbles
\	Block move, RAM-to-RAM
HHHH ?	Split RAM data about center point
HHHH >	Shuffle RAM data about center point

Programmer Responses

>	Prompt character
F	Fail character
?	Command to programmer not understood

Terminal Remote Control

Control Key Commands

ESC	Abort a command
BREAK	Abort binary transfer
SPACE	Re-execute D, I and C commands
LINE FEED	Display the last-executed command
RETURN	Execute a command or re-execute a previous command

Device Commands

CD	Clear Device Counter
SP	Device size
FP	Inquire Family/Pinout (UniPak only)
FY FF/PP	Select Family "FF" and Pinout "PP" (UniPak only)
PO PP	Select Pinout "PP" (UniPak only)
LD	Load
PG	Program
VF	Verify

Utility Commands

KF A/D	Keyboard format
CN	Software configuration number
NM	Nibble mode
BM	Byte mode
SM	Size memory
SF SC	External function
SC	Sum-check
CC	No-operation command
ZP	Exit Remote Control

Editing Commands

CM	Complement memory
CA	Clear all RAM
SN	Swap nibbles
SD	Split RAM data about center point
SH	Shuffle RAM data about center point
BL	RAM-to-RAM block move
MM	Enter Memory Mode
MO	Terminal enters Memory Mode at the last displayed address

I/O Commands

D	Select odd parity
E	Select even parity
N	Select no parity
J	Set one stop bit
K	Set two stop bits
HH M	Select record size
HH U	Set nulls
HHHH W	Set Address Offset
FC A	Select translation format code
=	Disable 25 second timeout
I	Input data from computer to RAM
O	Output data from RAM to computer
C	Compare data in RAM with computer data
Y	Parity-error inquiry

Editing Commands

Q	Swap nibbles
\	Block move, RAM-to-RAM
HHHH ?	Split RAM data about center point
HHHH >	Shuffle RAM data about center point

Programmer Responses

>	Prompt character
F	Fail character
?	Command to programmer not understood

Terminal Remote Control

Control Key Commands

ESC	Abort a command
BREAK	Abort binary transfer
SPACE	Re-execute D, I and C commands
LINE FEED	Display the last-executed command
RETURN	Execute a command or re-execute a previous command

Device Commands

CD	Clear Device Counter
SP	Device size
FP	Inquire Family/Pinout (UniPak only)
FY FF/PP	Select Family "FF" and Pinout "PP" (UniPak only)
PO PP	Select Pinout "PP" (UniPak only)
LD	Load
PG	Program
VF	Verify

Utility Commands

KF A/D	Keyboard format
CN	Software configuration number
NM	Nibble mode
BM	Byte mode
SM	Size memory
SF SC	External function
SC	Sum-check
CC	No-operation command
ZP	Exit Remote Control

Editing Commands

CM	Complement memory
CA	Clear all RAM
SN	Swap nibbles
SD	Split RAM data about center point
SH	Shuffle RAM data about center point
BL	RAM-to-RAM block move
MM	Enter Memory Mode
MO	Terminal enters Memory Mode at the last-displayed address

I/O Commands

OP	Odd parity
EP	Even parity
NP	No parity
DP	Default parity
ND NN	Null define
RS RR	Record size
OS	Select one stop bit
TS	Select two stop bits
DS	Default stop bits
FM FC	Translation format
VM AAAA	Virtual Memory Offset
DT	Disable timeout
DI	Data input
DO	Data output
DC	Data compare
QA	Parameters inquiry
QB	Input-compare errors inquiry
QC	Input-buffer overflow errors inquiry
QD	Data transfer errors inquiry

Memory Mode Commands

N	Display next address
L	Display last address
J	Jump address
C	Change data
I	Insert data
D	Delete data
R	Repeat data
F	Fill data
U	Fill unprogrammed data
S	Search data
B	Substitute data
T	List
E	Escape Memory Mode

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System 19 Errors

ERR	
21	System PROM sum-check error
22	Illegal bit error
23	Programming error
24	First pass verify error
25	Second pass verify error
26	No Programming Electronics installed
27	Programming Electronics reset
28	L1 plus L2 greater than RAM
30-39	Calibrate mode address range error
41	Programming Electronics error
42	Framing error
43	Overrun error
46	Framing and overrun error
48	I/O timeout (25 sec.)
50	Serial port buffer overflow
52	No data input
54	Input compare error
56	Insufficient data on remote input
57	Address range error
61	Too much data
62	No RAM installed
63	Last RAM address not on 1K boundary
64	RAM write failure
65	RAM data failure
66	Program memory failure
68	Unidentified interrupt
70-79	Data locked
81	Programming Electronics error
82	Parity error
84	Sum-check error
83	Invalid data
85	Composite error (81 and 82)
86	Composite error (81 and 84)
87	Composite error (82 and 84)
91	Composite error (81, 82 and 84)
92	Address-field error
93	Address-check error
94	Record-count error
95	Record-type error
96	Illegal split or shuffle
97	Illegal center point
98	Block-move parameters out of range
	L2 plus L3 greater than device

Programming Electronics Errors

IFL (Series 28) Programming Pak, 919-1542 (Signetics)

22	Programming error
25	No Pak or socket adapter installed
31	Excessive current drain
32	Backwards device
33	Programming Pak write error
37	Illegal RAM data
38	Calibration error

FPLA Programming Pak, 919-1549 (Fairchild)

31	Excessive current drain
32	Backwards device
33	Programming Pak write error
37	Illegal RAM data
38	Illegal operation during calibration

Addressable I/O Port Programming Pak, 919-1586

31	Excessive current drain
32	Backwards device
34	Wrong socket adapter
35	Multiple enables
36	No enables
37	Protect-programming failure
38	Illegal operation during calibration
39	Wrong bit programmed

I/O Commands

OP	Odd parity
EP	Even parity
NP	No parity
DP	Default parity
ND NN	Null define
RS RR	Record size
OS	Select one stop bit
TS	Select two stop bits
DS	Default stop bits
FM FC	Translation format
VM AAAA	Virtual Memory Offset
DT	Disable timeout
DI	Data input
DO	Data output
DC	Data compare
QA	Parameters inquiry
QB	Input-compare errors inquiry
QC	Input-buffer overflow errors inquiry
QD	Data transfer errors inquiry

Memory Mode Commands

N	Display next address
L	Display last address
J	Jump address
C	Change data
I	Insert data
D	Delete data
R	Repeat data
F	Fill data
U	Fill unprogrammed data
S	Search data
B	Substitute data
T	List
E	Escape Memory Mode

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Array Size Technology	PROM Part Number	Family Code	Pinout Code
Advanced Micro Devices			
32x8 FL	27S08/LS08	15	02
32x8 FL	27S09/LS09	15	02
32x8 FL	27S18/29750A	16	02
32x8 FL	27S19/29751A	16	02
256x4 FL	27S10/LS10	15	01
256x4 FL	27S11/LS11	15	01
256x4 FL	27S20/29760A	16	01
256x4 FL	27S21/29761A	16	01
512x4 FL	27S12/29770	16	03
512x4 FL	27S13/29771	16	03
512x8 FL	27S28	16	09
512x8 FL	27S29	16	09
512x8 FL	27S30	16	36
512x8 FL	27S31	16	36
1024x4 FL	27S32	16	38
1024x4 FL	27S33	16	38
1024x8 FL	27S180	16	37
1024x8 FL	27S181	16	37
2048x4 FL	27S184	16	06
2048x4 FL	27S185	16	06
1024x8 MOS	2708	●21	27
2048x8 MOS	4716	●19	23
Electronic Arrays			
1024x8 MOS	2708	●21	27
2048x8 MOS	2716	●19	23
Fairchild Semiconductor			
256x4 FL	93417	01	01
256x4 FL	93427	01	01
512x4 FL	93436	01	03
512x4 FL	93446	01	03
512x8 FL	93438	01	15
512x8 FL	93448	01	15
1024x4 FL	93452	01	05
1024x4 FL	93453	01	05
1024x8 FL	93450/936450	01	16
1024x8 FL	93451/936450	01	16
1024x8 FL	93460	01	16
1024x8 FL	93461	01	16
1024x8 MOS	2708	●21	27
Fujitsu			
1024x8 MOS	8518 (2708)	●21	27
2048x8 MOS	8516 (2716)	●19	23
Harris Semiconductor			
32x8 FL	7602	05	02
32x8 FL	7603	05	02
256x4 FL	7610	05	01
256x4 FL	7611	05	01
Harris Semiconductor			
256x8 FL	7629	05	43
512x4 FL	7620	05	03
512x4 FL	7621	05	03
512x8 FL	7640	05	15
512x8 FL	7641	05	15
512x8 FL	7648	05	09
512x8 FL	7649	05	09
1024x4 FL	7642	05	05
1024x4 FL	7643	05	05
1024x4 FL	7644	05	04
1024x8 FL	7608	05	16
1024x8 FL	7680	05	16
1024x8 FL	7681	05	16
2048x4 FL	7684	05	06
2048x4 FL	7685	05	06
2048x4 FL	7686	05	10
2048x4 FL	7687	05	10
2048x8 FL	76160	05	21
2048x8 FL	76161	05	21
2048x8 FL	7616	05	42

Array Size Technology	PROM Part Number	Family Code	Pinout Code
Hitachi			
2048x8 MOS	462716	19	23
2048x8 MOS	48016	●33	23
4096x8 MOS	46532	●19	25
4096x8 MOS	46732	●19	24
Intel			
512x8 MOS	2704/8704	●21	26
1024x8 MOS	2708/8708	●21	27
1024x8 MOS	2758	●19	22
1024x8 MOS	2758 S1865	●19	35
2048x8 MOS	2716	●19	23
4096x8 MOS	2732	●19	24
4096x8 MOS	2732A	●27	24
8192x8 MOS	2764	●35	33
Mitsubishi			
1024x8 MOS	58732S(2708)	●21	27
1024x8 MOS	2708	●21	27
2048x8 MOS	2716	●19	23
Monolithic Memories			
32x8 FL	5330/6330	29	02
32x8 FL	5331/6331	29	02
256x4 FL	5300/6300	11	01
256x4 FL	5301/6301	11	01
256x8 FL	5335/6335	11	14
256x8 FL	5336/6336	11	14
256x8 FL	5308/6308	11	08
256x8 FL	5309/6309	11	08
512x4 FL	5305/6305	11	03
512x4 FL	5306/6306	11	03
512x8 FL	5340/6340	11	15
512x8 FL	5341/6341	11	15
512x8 FL	5348/6348	11	09
512x8 FL	5349/6349	11	09
1024x4 FL	5352/6352	11	05
1024x4 FL	5353/6353	11	05
1024x8 FL	5380/6380	11	16
1024x8 FL	5381/6381	11	16
256x4 FL	63S/63LS/63PS140	18	01
256x4 FL	63S/63LS/63PS141	18	01
512x4 FL	63S/63LS/63PS240	18	03
512x4 FL	63S/63LS/63PS241	18	03
512x8 FL	63S/63LS/63PS480	18	09
512x8 FL	63S/63LS/63PS481	18	09
1024x4 FL	63S/63LS/63PS440	18	05
1024x4 FL	63S/63LS/63PS441	18	05
1024x4 FL	63RS/63RA441	18	07
2048x4 FL	63RA/63RS841	18	11
Mostek			
2048x8 MOS	2716	●19	23
Motorola			
512x4 FL	7620	05	03
512x4 FL	7621	05	03
512x8 FL	7640	05	15
512x8 FL	7641	05	15
1024x4 FL	7642	05	05
1024x4 FL	7643	05	05
1024x8 FL	7680	05	16
1024x8 FL	7681	05	16
2048x4 FL	7684	05	06
2048x4 FL	7685	05	06
1024x8 MOS	68708/2708L	●21	27
1024x8 MOS	2708P	●21	27
2048x8 MOS	TMS 2716	●23	28
2048x8 MOS	MCM 2716	●19	23
4096x8 MOS	2532	●19	25

Array Size Technology	PROM Part Number	Family Code	Pinout Code
National Semiconductor			
32x8 FL	54/74S188	08	02
32x8 FL	54/74S288	08	02
256x4 FL	54/74S387	08	01
256x4 FL	54/74S287	08	01
512x4 FL	54/74S570	08	03
512x4 FL	54/74S571	08	03
512x8 FL	74S475/77/87S295	08	15
512x8 FL	74S474/77/87S296	08	15
512x8 FL	54/74S473	08	09
512x8 FL	54/74S472	08	09
1024x4 FL	54/74S572	08	05
1024x4 FL	54/74S573	08	05
1024x4 FL	54/74S574	08	34
1024x8 FL	87S180	08	16
1024x8 FL	87S181	08	16
2048x4 FL	87S184	08	06
2048x4 FL	87S185	08	06
2048x8 FL	87S190	08	21
2048x8 FL	87S191	08	21
1024x8 MOS	2708	●21	27
2048x8 MOS	2716	●19	23
4096x8 MOS	2532	●19	25
4096x8 MOS	2732	●19	24
Nippon Electric Co., Ltd.			
2048x8 MOS	2716	●19	23
Oki			
2048x8 MOS	2716	●19	23
Raytheon			
256x4 FL	29660/62	11	01
256x4 FL	29661/63	11	01
256x8 FL	29600/02	11	08
256x8 FL	29601/03	11	08
512x4 FL	29610/12	11	03
512x4 FL	29611/13	11	03
512x8 FL	29620/22	11	09
512x8 FL	29621/23	11	09
512x8 FL	29624/26	11	15
512x8 FL	29625/27	11	15
1024x4 FL	29640/42	11	05
1024x4 FL	29641/43	11	05
1024x8 FL	29634/36	11	16
1024x8 FL	29635/37	11	16
1024x8 FL	29630/32	11	16
1024x8 FL	29631/33	11	16
2048x4 FL	29650/52	11	06
2048x4 FL	29651/53	11	06
2048x8 FL	29680/82	11	21
2048x8 FL	29681/83	11	21
Signetics			
32x8 FL	82S23	10	02
32x8 FL	82S123	10	02
256x4 FL	82S126	10	01
256x4 FL	82S129	10	01
512x4 FL	82S130	10	03
512x4 FL	82S131	10	03
512x8 FL	82S140	10	15
512x8 FL	82S141	10	15
512x8 FL	82S146	10	09
512x8 FL	82S147	10	09
1024x4 FL	82S136	10	05
1024x4 FL	82S137	10	05
1024x8 FL	82S/LS180	10	16
1024x8 FL	82S/LS181	10	16
1024x8 FL	82S182	10	16
1024x8 FL	82S183	10	16
1024x8 FL	82S2708	10	16
2048x4 FL	82S184	10	06
2048x4 FL	82S185	10	06
2048x8 FL	82S190	10	21
2048x8 FL	82S191	10	21
1024x8 MOS	2708	●21	27

Array Size Technology	PROM Part Number	Family Code	Pinout Code
Texas Instruments			
32x8 FL	74188A	04	02
32x8 FL	18SA030 (54/74S188)	04	02
32x8 FL	18S030 (54/74S288)	04	02
256x4 FL	14SA10 (54/74S387)	03	01
256x4 FL	14S10 (54/74S287)	03	01
256x4 FL	24S10	13	01
256x4 FL	24SA10	13	01
256x8 FL	18SA22 (54/74S470)	04	08
256x8 FL	18S22 (54/74S471)	04	08
512x8 FL	18SA42 (54/74S473)	04	09
512x8 FL	18S42 (54/74S472)	04	09
512x8 FL	18SA46 (54/74S475)	04	15
512x8 FL	18S46 (54/74S474)	04	15
512x8 FL	28S42	13	09
512x8 FL	28L42	13	09
512x8 FL	28P42	13	09
1024x4 FL	24SA41 (54/74S477)	13	38
1024x4 FL	24S41 (54/74S476)	13	38
1024x8 FL	28SA86 (54/74S479)	13	16
1024x8 FL	28S86 (54/74S478)	13	16
1024x8 FL	28L86 (54/74LS478)	13	16
1024x8 FL	28S2708 (54/74S2708)	13	16
2048x4 FL	24S81 (74S454)	13	06
2048x4 FL	24SA81 (74S455)	13	06
2048x8 FL	28S166	13	21
2048x8 FL	28L166	13	21
1024x8 MOS	2508	●19	22
1024x8 MOS	2708/27L08	●21	27
2048x8 MOS	2716	●23	28
2048x8 MOS	2516	●19	23
4096x8 MOS	2532	●19	25
8192x8 MOS	2564	●31	30
Toshiba			
512x8 MOS	321	●21	26
1024x8 MOS	322	●21	27
2048x8 MOS	323	●19	23

NOTE

This list may not include the latest additions to the MOS Pak and UniPak capabilities. Add new PROMs below

Array Size Technology	PROM Part Number	Family Code	Pinout Code

SECTION 1
INTRODUCTION

1.1 OVERVIEW

Data I/O's UniPak™ reliably programs over 400 popular MOS and bipolar devices. Values for programming variables, including pinouts, voltage levels and timing, are stored in firmware tables. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM. This method allows high-speed operation with minimum firmware overhead. The UniPak™ is designed to adapt to the programming requirements of many different devices. Pinout variations are handled by seven device sockets on the UniPak™ and, in some cases, by adapters which connect to socket 1 or 2. Specially designed electronic switches allow programming of both bipolar and MOS devices.

To maximize control speed during programming, the UniPak™ makes extensive use of addressable latches for control signals. For flexibility in waveform generation, digital-to-analog converters (DACs) control all major power supplies, with several rise and fall times selected by firmware.

1.2 PROGRAMMER COMPATIBILITY

Before using the -007 version of the UniPak™, read the information in this section to be sure your programmer does not require a modification. Either or both of two modifications to your System 17 or 19 may be required for compatibility with the -007 or later version of the UniPak™:

A. It may be necessary to make a small hardware modification to the System 17/19 Controller (702-1520).

B. A firmware update may be necessary.

29A Universal Programmers and 100A Production Programmers may need firmware updates.

1.2.1 Hardware Modification

System 19s with serial numbers below 1516 and System 17s with serial numbers below 219 will require small modifications for use with the UniPak™. The UniPak™ may cause error messages which are invalid if the modification is not made. No other programmer functions are affected, nor will attempting an operation harm the programmer, the UniPak™, or a device in the socket.

CAUTION

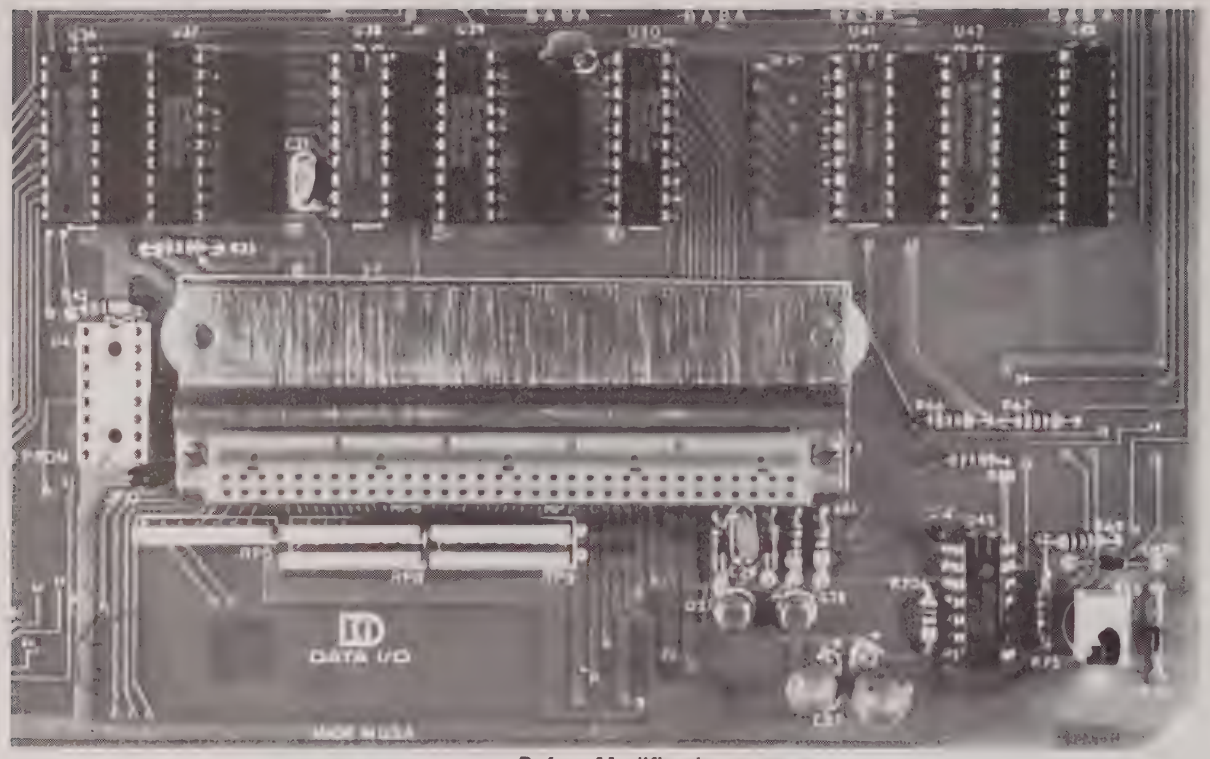
The following hardware modification to the System 17 and 19 should be performed by a qualified technician only. If the facilities are not available to perform the modification, contact your local Data I/O Service Center. A list of all Data I/O service centers is located in the back of this manual.

Modification Instructions

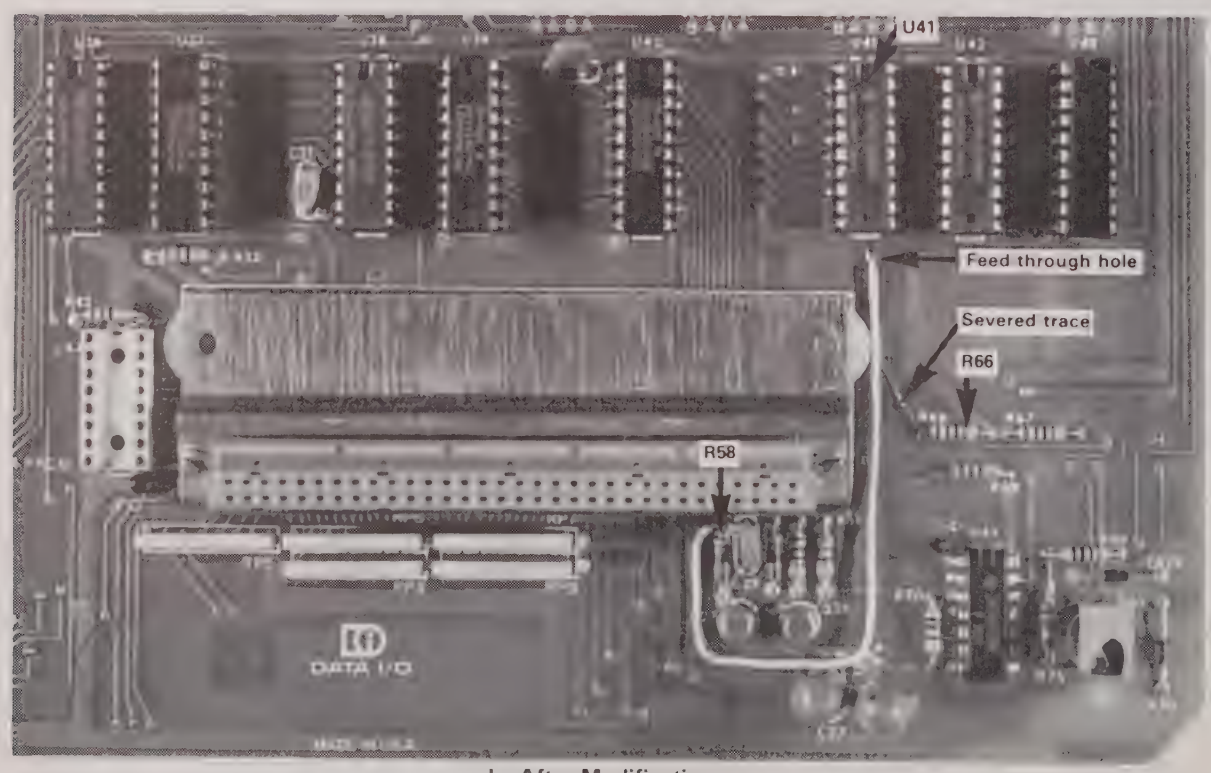
1. Unplug power cord.
2. Remove Programming Pak.
3. Remove protection shield.
   a. Pull the two snap-lock connectors and lift them gently.
   b. Lift the back edge of the plate first and pull it up slightly and turn it to the left until it is clear.
4. Remove top cover.
   a. Turn the programmer on its top.
   b. Remove the four cover screws.
   c. Turn the programmer upright and lift the cover off.
5. Remove display panel.
   a. Remove four screws located at the corner of the display panel.
   b. Remove the screw fastening the support bracket to the power supply assembly.
   c. Remove the screw fastening the support bracket to the front of the base.
   d. If there is a screw fastening the support bracket to the bottom plate, remove it.
6. Refer to figure 1-1. Sever the trace connecting R66 to U41 pin 1 just above R66 (left side).
7. Install an insulated wire from the top side of R58 (just *left* of C29, in front of the Programming Pak connector) to U41 pin 1. To connect to U41 pin 1, use the feed-through hole on the trace tying R66 to U41. (See figure 1.)
8. Reinstall the display panel top cover and protective shield by reversing the removal procedures.

Programmer Check

9. Install a Programming Pak.
   a. Check the programmer for proper initialization.
   b. Load a device with a known data pattern and perform a verify to confirm proper operation.



a. Before Modification



b. After Modification

Note: Your controller may appear slightly different. Be sure connections are made to the components designated in this bulletin.

Figure 1-1. Jumper-Wire Location on Programmer Controller, 702-1520

1.2.2 Software Update

Some programmers require a software update for compatibility with the -004 or later version of the UniPak™. Table 1-1 shows the revisions and software configuration-check numbers for each programmer configuration requiring a software update. If your System 17, 19, 29A or 100A is one of these revisions, contact a Data I/O sales representative to order the appropriate update kit.

To determine the revision level of a programmer, follow the procedure below to display the software configuration-check number and compare it to table 1-1.

- **System 19 and 29A, all configurations:** Key in Select Code B2-START.
- **System 29B, all configurations:** Key in Select Code B2-START. (All configurations are compatible.)
- **100A Production Programmer:** Key in Select Code 10.
- **System 1730:** Enter remote control and use the G command.
- **System 1731:** Enter remote control and use the CN command.

1.3 APPLICATIONS

Table A-1 lists all the devices that could be programmed with the UniPak™ when this manual was published. In many cases when a new device with industry-standard pinout is introduced within a manufacturer's family, the UniPak™ WILL NOT require a revision to program it. For some new applications, such as to accommodate a new device family, a firmware update of the UniPak™ may be required. The revision number is stamped after the part number (950-0099) along the underside of the top edge of the UniPak™ socket assembly.

1.4 SPECIFICATIONS

The UniPak™ receives its power from the programmer mainframe. Programming waveforms are generated from raw programmer supplies using regulators controlled by the programmer's microprocessor. The controlling firmware is located on a circuit card within the UniPak™.

The physical and environmental specifications are:

- Altitude: Sea level to 3 km (10,000 ft.)
- Dimensions: 20.9 x 17.0 x 10.5 cm (8.2 x 6.7 x 4.2 in.)
- Humidity (operating): 90% maximum (noncondensing)
- Humidity (storage): 95% maximum (noncondensing)
- Temperature (operating): 0 to 40°C (32 to 104°F)
- Temperature (storage): −40 to 55°C (−40 to 131°F)
- Weight: 1.38 kg (3 lb. 0.5 oz.)

Table 1-1. Programmers Requiring Updates

System	Revision	Software Configuration Check Number
990-1900	A	F9CF
	B	ØØAC
	C	Ø7CD
	D	ØB11
	E	FC6A
	F	B16C
990-1901	A	89CC
	B	CC89
	C	6BCD
990-1902	A	C56C
	B	8B82
	C	9141
	D	9ØØ2
	E	2Ø68
	F	29CE
	G	3868
	H	3599
990-1903	A	2C23
	B	6A9B
	C	3A33
990-1730	A	6D7B
	B	ADF5
	C	35EE
	D	4180
	E	44F8
990-1731	A	93AA
	B	3A3A
29A	A	1ECA
	B	20A4
29A w/computer remote control	A	BB41
	B	CØØB
100A	A	917F
	B	9405
	C	9DEE
	D	9BED

1.5 FIELD APPLICATIONS SUPPORT

Data I/O has field applications engineers (FAE's) throughout the world. They can provide additional information about interfacing Data I/O products with other equipment and answer questions about equipment. FAE's are located within the United States at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of one year, unless specified otherwise, begins when you receive the equipment. The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O service center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs, but also calibration of all Data I/O products. A list of all Data I/O service centers is located in the back of this manual.

1.8 ORDERING

To order equipment, contact your Data I/O sales representative. Orders must contain the following information:

- Description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- Quantity of each item ordered
- Shipping and billing address of firm, including ZIP code
- Name of person ordering equipment
- Purchase order number
- Desired method of shipment

SECTION 2
INSTALLATION

2.1 INSPECTION

Your UniPak™ was tested both electrically and mechanically before it was shipped, and was carefully packaged to prevent shipping damage. It should, therefore, arrive free of any defect, without marks or scratches, and in perfect operating condition. However, carefully inspect the instrument for any damage that may have occurred in transit. If you note any damage, file a claim with the carrier and notify Data I/O.

2.2 UniPak™ INSTALLATION

The UniPak™ may be installed and removed with the programmer's power on; this feature allows you to retain data in RAM during module changes. If the programmer power is turned on before the UniPak™ is installed, you will hear a beep until the UniPak™ is installed.

NOTE

Voltage transients can cause device damage. Thus, be sure that all sockets are empty when:

- *switching power on or off*
- *installing or removing the UniPak™*

To install the UniPak™, do the following:

1. Slide the UniPak™ into the opening in the programmer (figure 2-1).
2. Tilt the UniPak™ up and gently push it back to hook the flange of the UniPak™ over the back edge of the programmer opening (figure 2-1, a).
3. Lower the UniPak™ into position as shown in figure 2-1, b.
4. Press gently on the front edge of the UniPak™ to ensure a good connection (figure 2-1, c).

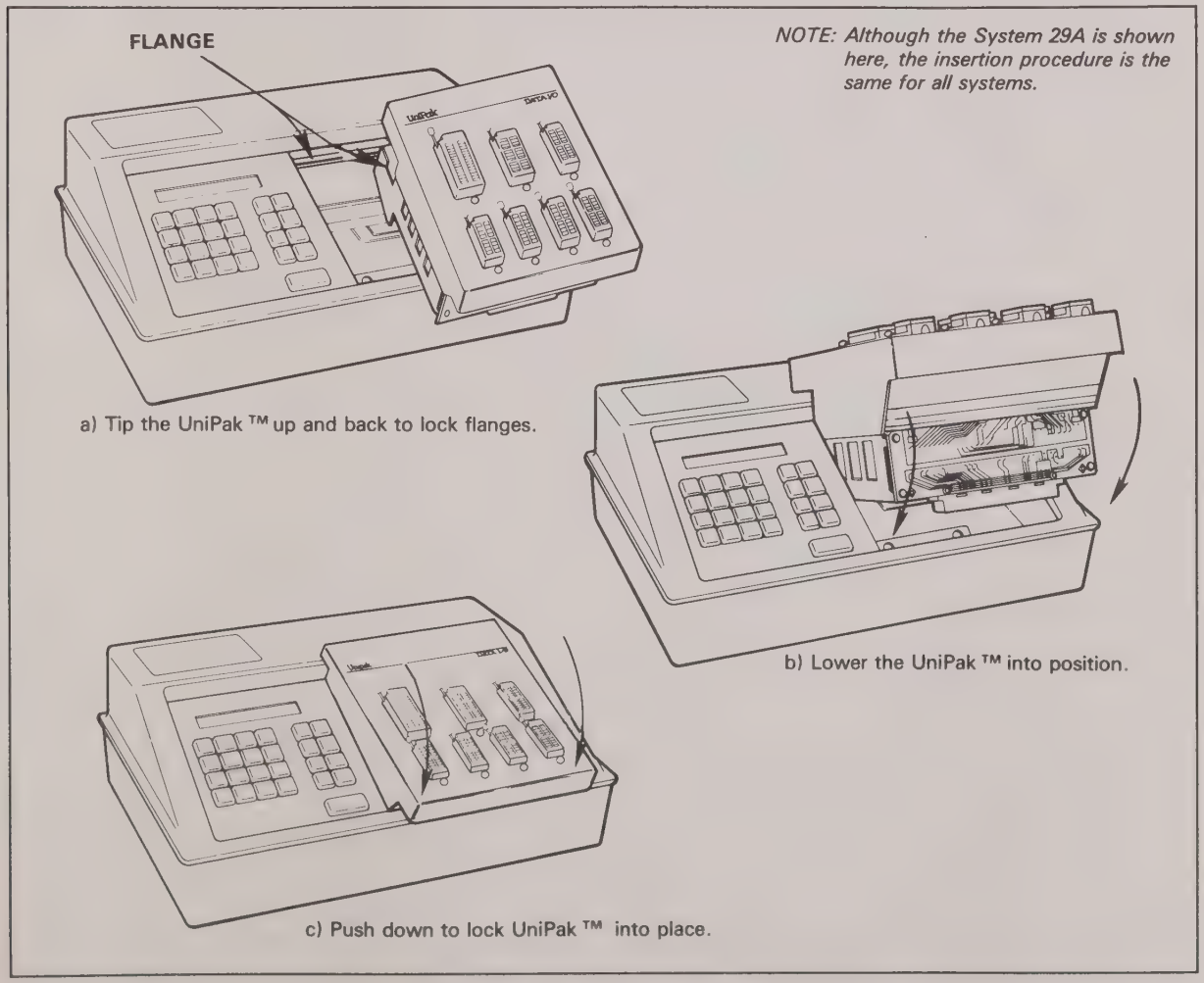

FLANGE
NOTE: Although the System 29A is shown here, the insertion procedure is the same for all systems.
a) Tip the UniPak ™ up and back to lock flanges.
b) Lower the UniPak ™ into position.
c) Push down to lock UniPak ™ into place.

Figure 2-1. UniPak™ Installation

2.3 UniPak™ REMOVAL

1. Check to make sure the programmer is not in the process of an operation. If it is, wait until the operation is complete (the action symbol on the display disappears).
2. Check to make sure a device is not in a socket. If one is in a socket, remove it as described in section 3.7.
3. Tilt the UniPak™ up and gently remove it from the programmer.

2.4 REPACKING FOR SHIPMENT

If the UniPak™ is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and name. If the original shipping container is to be used, place the UniPak™ in the container with the appropriate packing material and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3
OPERATION

3.1 OVERVIEW

The UniPak™ can be used in 29A, 29B, System 19, or 100A programmers of any configuration; see section 1.2 for firmware revision levels required. The typical programming operation with a 29A programmer and a UniPak™ is illustrated in figure 3-1. As can be seen from this figure, the UniPak™ can obtain data from three sources (a master device, a serial port, or the keyboard). Because the serial port and keyboard operations are unique for each type of programmer, you will be referred to your 29A, 29B, System 19, or 100A programmer manual for details on how to program using these mainframes.

When using a master device as the data source to program a blank device, you must first instruct the programmer to copy the device data into programmer RAM (shown as COPY in figure 3-1 and described in section 3.4). Then enter the family code and pinout code as described in section 3.5. The data in the device will have been copied to the RAM of your 29A when you press START, as shown in figure 3-1. You must then remove the master device and instruct the programmer to copy the information just stored in its RAM to a blank device. This completes the basic programming operation.

The procedures to perform basic operations with your UniPak™ are described in this section. You should follow these procedures to properly operate your UniPak™. Wherever possible, key sequences have been included for using your UniPak™ with a 29A Universal Programmer with Rev C firmware (read section 1.2 carefully to determine your programmer's firmware revision level). Refer to your programmer manual for key sequences for the System 19, 29B, and 100A programmers.

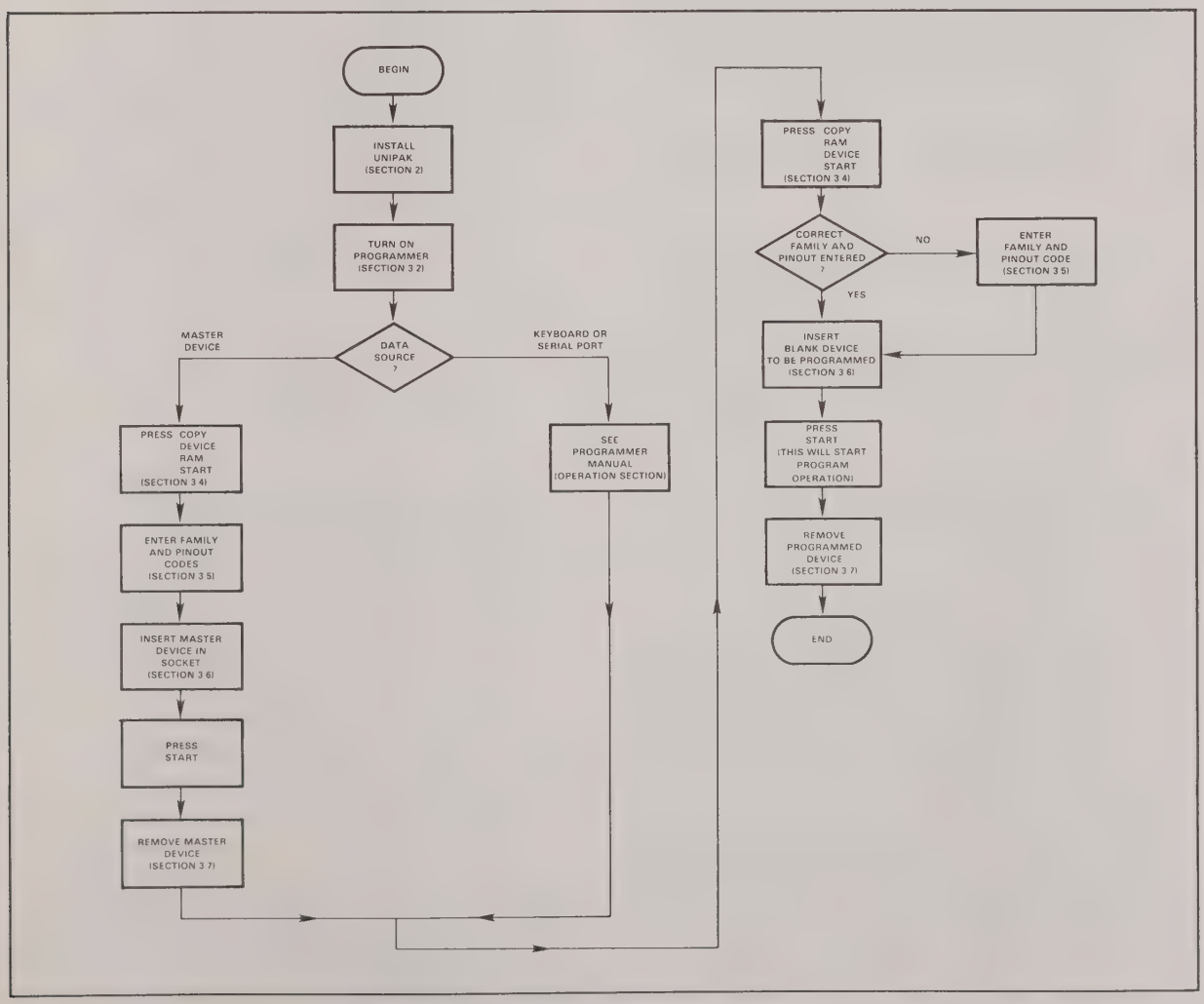

BEGIN
INSTALL UNIPAK (SECTION 2)
TURN ON PROGRAMMER (SECTION 3.2)
DATA SOURCE ?
MASTER DEVICE
KEYBOARD OR SERIAL PORT
PRESS COPY DEVICE RAM START (SECTION 3.4)
ENTER FAMILY AND PINOUT CODES (SECTION 3.5)
INSERT MASTER DEVICE IN SOCKET (SECTION 3.6)
PRESS START
REMOVE MASTER DEVICE (SECTION 3.7)
SEE PROGRAMMER MANUAL (OPERATION SECTION)
PRESS COPY RAM DEVICE START (SECTION 3.4)
CORRECT FAMILY AND PINOUT ENTERED ?
NO
ENTER FAMILY AND PINOUT CODE (SECTION 3.5)
YES
INSERT BLANK DEVICE TO BE PROGRAMMED (SECTION 3.6)
PRESS START (THIS WILL START PROGRAM OPERATION)
REMOVE PROGRAMMED DEVICE (SECTION 3.7)
END

Figure 3-1. Typical 29A Programmer Operation

3.2 POWER UP

NOTE

If the UniPak™ is not installed in the programmer before power is turned on, you will hear a beep until the UniPak™ is installed.

When turned on, the programmer will perform an automatic self-test routine. When the self-test routine is complete, the programmer will signal its readiness.

To turn the programmer on, do the following:

1. Check to make sure a device is not in a socket. If a device is in a socket, lift up the lever (located on the upper left of the socket; see section 3.7), then gently lift the device out of the socket.
2. Plug the AC power cord into the power outlet.
3. Flip the power switch up to the "ON" position (see figure 3-2).

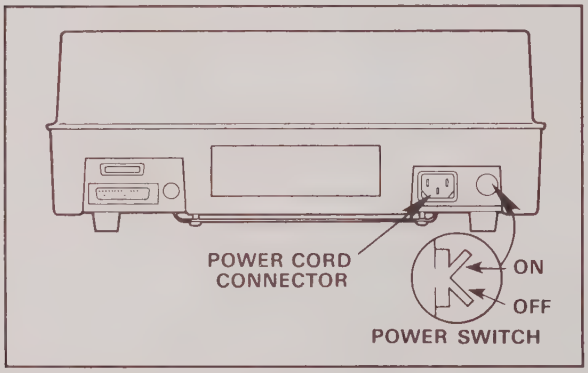


Figure 3-2. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off, do the following procedure:

1. Check to make sure that the programmer is not in the middle of an operation. If it is, wait until that operation is through.
2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.7.
3. Flip the power switch down to the "OFF" position (figure 3-2).

3.4 BASIC OPERATION

All data transfer or verification operations take place between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the procedure to transfer data via a serial port varies from programmer to programmer, this manual describes only data transfer with the 29A. For other programmers, refer to your programmer operation manual.

The basic data transfer operations that can be performed with the UniPak™ and the 29A Universal Programmer are:

- Load RAM with data from a master device (described in section 3.4.1).
- Verify RAM data against the device data (described in section 3.4.2).
- Program a device with RAM data (described in section 3.4.3).

3.4.1 Load RAM With Data From Master Device

To load the 29A RAM with data from a master device, follow the steps listed below.

1. Press COPY; 29A displays COPY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE

The device is the source of data.

3. Press RAM; 29A displays CO DEV > RAM ∧ ADDR

NOTE

The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3.5).
6. Insert the master device into the UniPak™ (see section 3.6).
7. Press START; 29A displays LOADING DEVICE
   LOAD DONE XXXX

NOTE

XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak™ (see section 3.7).

During source destination operations (copy and verify), ADDR and SIZE appear in the 29A prompts. These correspond to starting address and block size, respectively. For more detail on these parameters, see your programmer operation manual. When reading a device, the UniPak™ applies a nominal V_{CC} level. To simulate loading on device outputs, each output is driven by a 1.6 mA current source.

3.4.2 Verify RAM Data Against Master Device Data

The two-pass verify consists of comparing the device data to RAM data and is performed at two V_{CC} levels; these levels, plus the output-sink currents and the output-level-sense voltages, vary according to each manufacturer's requirements.

To verify that data entered in the 29A RAM duplicates the master device data, follow these steps:

1. Press VERIFY; 29A displays VERIFY DATA FROM
2. Press DEVICE; 29A displays DEV ∧ ADDR/SIZE TO

NOTE
The device is the source of data.

3. Press RAM; 29A displays VE DEV > RAM ∧ ADDR

NOTE
The RAM is the destination of the data from the master device.

4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3.5).
6. Insert the master device into the UniPak™ (see section 3.6).
7. Press START; 29A displays VERIFY DEVICE
   VE DEV DONE XXXX

NOTE
XXXX is the sumcheck of the device.

8. Remove the master device from the UniPak™ (see section 3-7).

3.4.3 Program Device With RAM Data

When programming a device, the system performs illegal-bit tests and blank checks at nominal V_{CC} and with nominal output loading.

To program a blank device with the data in the 29A RAM, follow these steps:

1. Press COPY; 29A displays COPY DATA FROM
2. Press RAM; 29A displays RAM ∧ ADDR/SIZE TO
3. Press DEVICE; 29A displays CO RAM > DEV ∧ ADDR
4. Press START; 29A displays FAM ∧ ØØ PIN ØØ
5. Enter the family code and pinout code (see section 3-5).
6. Insert the blank device into the UniPak™ (see section 3-6).
7. Press START; 29A displays TEST DEVICE
   PROGRAM DEVICE
   VERIFY DEVICE
   PRG DONE 01 XXXX
8. Remove the device from the UniPak™ (see section 3.7).

NOTE
XXXX represents the sumcheck of the device.

3.4.4 Extended Select Functions

In addition to the three basic source-destination functions (copy, verify and edit) and the select functions described in the Operation section of your programmer manual, the UniPak™ offers five extended select functions (CC, C3, CE, CF and EF). These functions are not required for normal operation of the UniPak™.

The extended select functions may be used from either the keyboard or from remote control.

Function CC displays the family and pinout codes of the last algorithm moved to RAM, usually the algorithm for the last device programmed or read.

To display the family and pinout codes of the last algorithm moved to RAM, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press CC START; 29A displays XXYY **

NOTE
XX represents the family code; YY represents the pinout code.

Function C3 gives access to options for specific family/pinout code combinations. If the UniPak™ is being used in a Model 19, this select code will work only from terminal remote or computer remote.

To enter the options, follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ∧
2. Press C3 START; 29A displays FXX PYY OPTIONS
3. Press START; 29A displays "NAME OF FIRST OPTION"

To select different options, press the REVIEW key. To execute an option, press START (in terminal remote, the RETURN key is used for the START key, and the space bar is used for the REVIEW key). If the option has subheadings under it, once the START key has been pressed, the REVIEW key can select the desired subheading. The START key is then pressed to execute the subheading. Once an option has been completely executed, an asterisk will be displayed after the option name. Complete execution may require doing a number of subheadings. Pressing the START key a second time after an option is completely executed will exit the options file, and the 29A will display OPTIONS DONE **.

NOTE

For the 8751H, the option "PROG SECTY ONLY" will program the security fuse as soon as the option is selected and executed.

Functions CE and CF are used to set the reject count (the number of programming pulses applied to a fuse or cell before it is rejected); CE sets the reject count back to the commercial specification (this is the default value) and CF sets the single-pulse reject count. This feature was accomplished in older UniPak™ models by adding 50 to the family code.

To select the commercial (default) reject count (CE), follow the procedure below.

1. Press SELECT; 29A displays SELECT CODE ^
2. Press CE START; 29A displays SELECT CODE **

To select the single-pulse reject count (CF), take the following steps:

1. Press SELECT; 29A displays SELECT CODE ^
2. Press CF START; 29A displays SELECT CODE **

Function EF calls up a four-digit hexadecimal configuration number and a two-digit decimal version number that correspond to the revision level and version number of the UniPak™ firmware. This function can be useful to identify firmware revision levels when communicating with Data I/O regarding field bulletins and updates.

To display the UniPak™ firmware configuration and version number, do the following:

1. Press SELECT; 29A displays SELECT CODE ^
2. Press EF START; 29A displays XXXX YY **

NOTE

XXXX represents the UniPak™ firmware configuration number, and YY represents the version number.

3.5 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the UniPak™ is specified by a unique combination of a two-digit family code and a two-digit pinout code (table A-1). Once the codes for a particular device are entered, the UniPak™ remains set up for any operation with that device until new codes are entered.

Your programmer manual will tell you where in the key sequence the family and pinout codes should be entered. If you enter invalid family and pinout codes, a beep will sound as you press either START or ENTER, or Err 30 (error 30) will be displayed and the operation will be aborted.

To select the family and pinout codes, procede as follows:

1. Locate the manufacturer name and part number stamped on the device.
2. Go to table A-1, column 1, and find the manufacturer's name.
3. Go to table A-1, column 3, entitled "PROM Part Number" and find the number corresponding to the number on the device.
4. Go to column 4 ("Family Code") and column 5 ("Pinout Code") to find the code numbers corresponding to the device number.
5. Enter the family and pinout codes you selected from table A-1.
6. Push "START."

NOTE

An LED (light-emitting diode) will light under one of the sockets.

Valid family and pinout codes must be in effect to use the System 19 DEVICE DATA key. When you press the DEVICE DATA key, either nominal, first-pass, or second-pass verify levels are applied to the device. The level applied depends on the System 19's position in executing the selected mode. If the KEYBD light is on, the nominal verify level is applied.

3.6 DEVICE INSERTION

Once you have chosen the appropriate family and pinout codes, the UniPak™ is ready to accept a device in the socket located above the lighted LED.

A good electrical connection between the device and the socket is essential. To ensure a good connection, do the following:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift up the lever on the upper left side of the socket above the lighted LED (see figure 3-3). The lever will stay locked in the upright position.
3. Gently insert the device in the socket above the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket, as shown in figure 3-3.
4. Push the lever down to lock the device in the socket.

Once you have entered the family and pinout codes, the UniPak™ is ready for device-related operations. The key sequence to load, program, and verify is described in the Operation section of your programmer manual.

3.7 DEVICE REMOVAL

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Flip up the lever on the left side of the socket (see figure 3-3). The lever will lock in the upright position.
3. Lift the device out of the socket; the LED will remain illuminated.

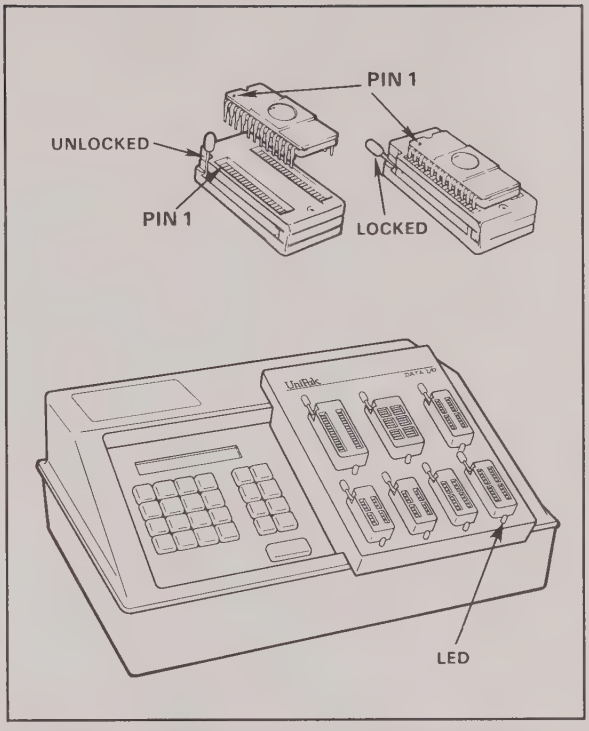


Figure 3-3. UniPak™ Sockets and Device Installation

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SECTION 4
MAINTENANCE/TROUBLESHOOTING/CALIBRATION

4.1 OVERVIEW

The support material in this section has been provided to help you keep your UniPak™ in good operating condition. General maintenance practices are discussed in section 4.2, while the basic troubleshooting steps are listed in section 4.3. For those UniPak™ users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams, are provided in section 4.4.

4.2 MAINTENANCE

Before the UniPak™ can be cleaned (section 4.2.2) and/or inspected (section 4.2.3), it must be disassembled as described below.

4.2.1 UniPak™ Disassembly

To disassemble the UniPak™, refer to figure 4-1 and follow the procedure outlined below.

1. Remove the UniPak™ from the programmer; see section 2.3 for details.
2. Place the UniPak™ face down on a flat surface.
3. Unscrew the captive fasteners (figure 4-1a) until they hang loosely; the screws will not separate from their standoffs.
4. Lift the card cage up slightly, then pull out (as shown in figure 4-1b) to unlock the flanges.

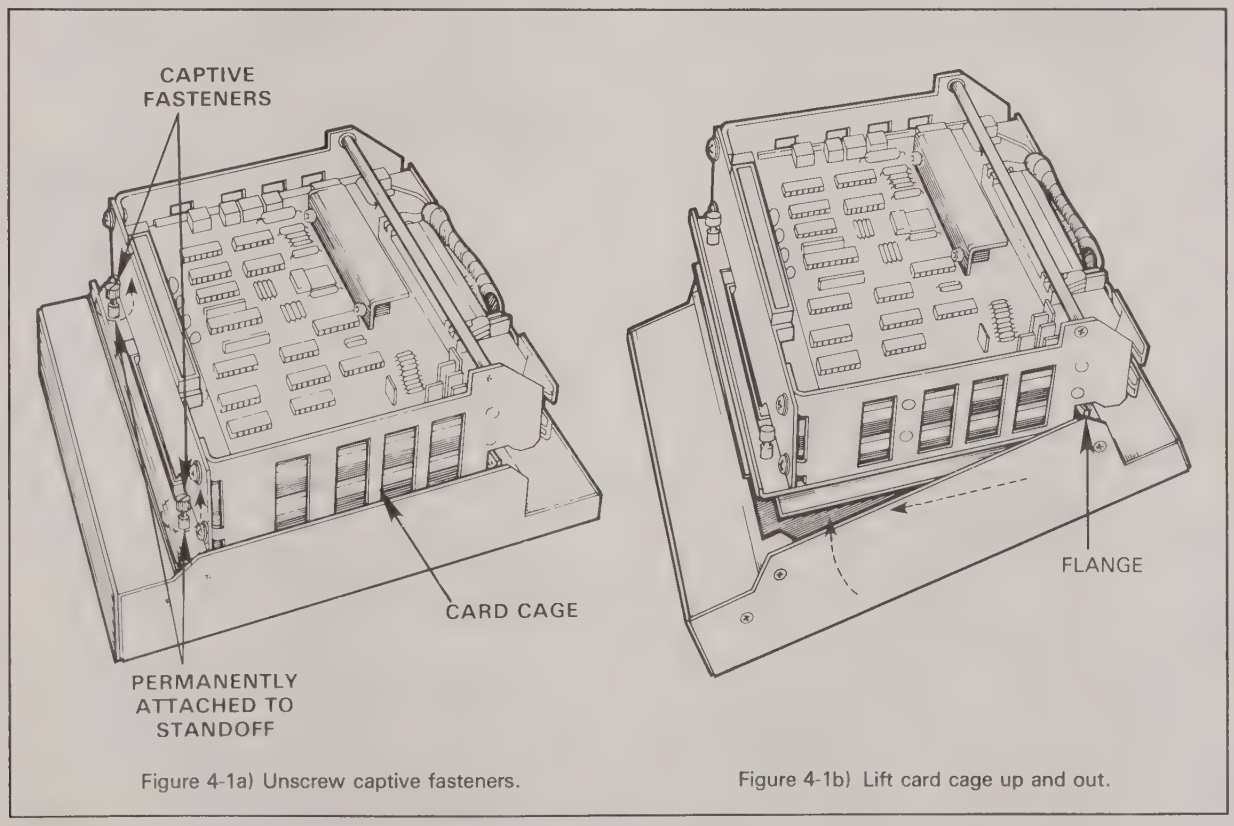


Figure 4-1a) Unscrew captive fasteners.

Figure 4-1b) Lift card cage up and out.

Figure 4-1. UniPak™ Disassembly

5. Lift the card cage up until you can see the socketboard interconnect cable and its connector (figure 4-2).
6. Flip the extraction tabs out on each side of the connector (figure 4-2).
7. Pull the cable out of the connector.
8. Flip the extraction tabs out on the top card (waveform generator card) and unplug the interconnect cable from its connector (figure 4-3).
9. Flip the extraction tabs out on the top card (waveform generator card).
10. Pull the waveform generator card out along the guides (figure 4-3).
11. Repeat steps 9, 10, and 11 for the extraction tabs on the address card.
12. Remove the two screws and the shield, and pull the memory card down to unplug it from the edge connector (as shown in figure 4-4).

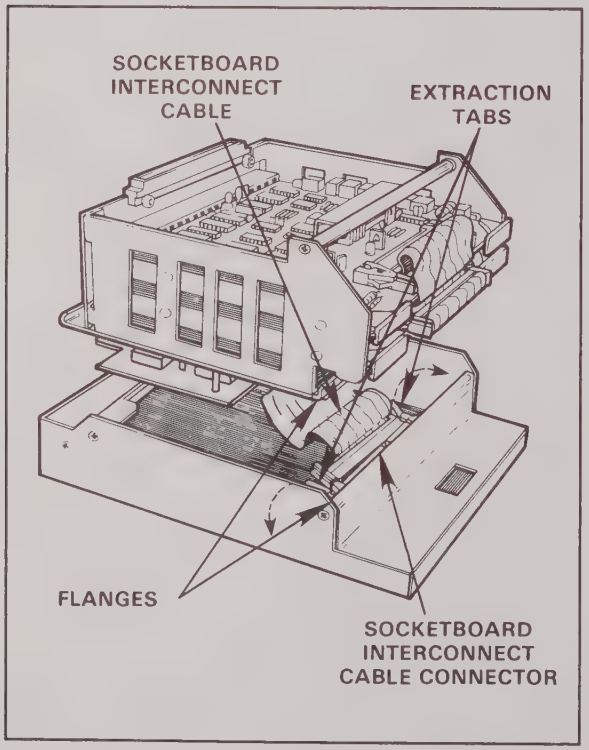


Figure 4-2. Socketboard Interconnect Cable Disconnect

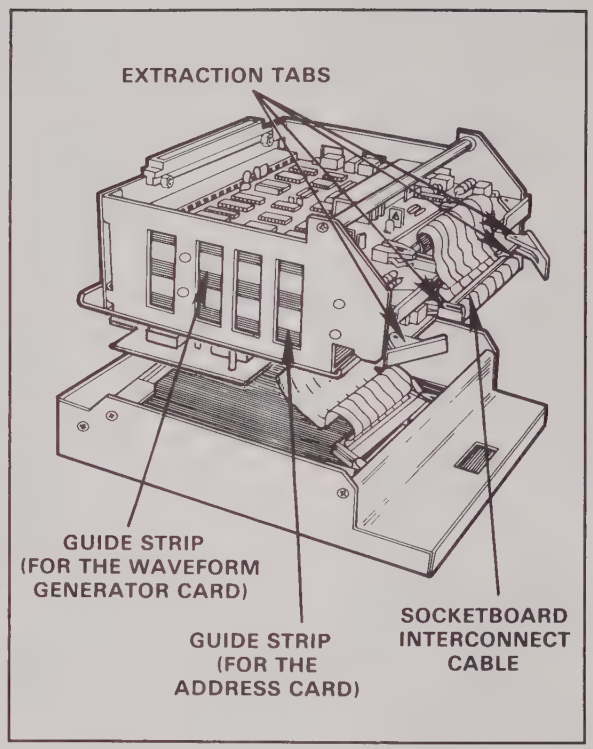

EXTRACTION TABS
GUIDE STRIP (FOR THE WAVEFORM GENERATOR CARD)
GUIDE STRIP (FOR THE ADDRESS CARD)
SOCKETBOARD INTERCONNECT CABLE

Figure 4-3. Circuit Board Removal

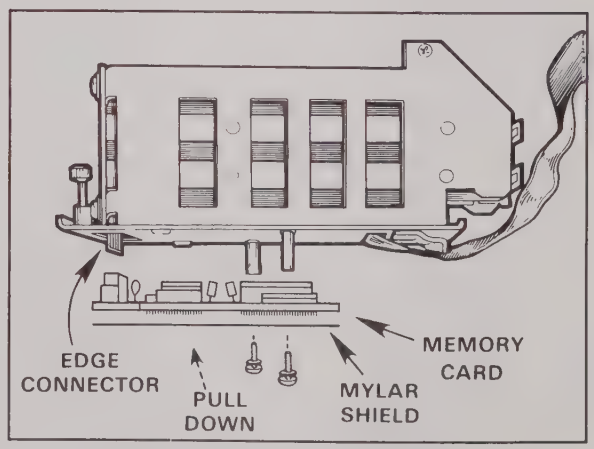


Figure 4-4. Memory Card Removal

4.2.2 Cleaning

Inspect the UniPak™ inside and out for accumulated dirt or dust. To clean the UniPak™, follow the procedure below.

1. Wipe any dust and/or dirt off the outside of the UniPak™ with a clean, damp cloth.

NOTE
Do not use abrasive cleaners or solvents. They will etch the paint.

2. Remove dust from the circuit boards with a blast of dry, compressed air or a clean, soft-bristled brush.

4.2.3 Inspection

You can help prevent malfunctions by periodically inspecting your UniPak™. Check cable connections, card seating, mounting of socketed components, etc., for shorts, opens or unstable continuity.

If you find heat-damaged components, be particularly careful to find and correct the cause of the overheating. This will prevent further damage.

4.2.4 UniPak™ Assembly

1. Plug the memory card onto its edge connector, as shown in figure 4-4.
2. Replace the shield, washers, and the two screws.
3. Flip the two extraction tabs down on the address card.
4. Using the flat surfaces of the extraction tabs, gently push the address card along the guides into its connector.
5. Make sure the extraction tabs on the interconnect cable connector are flipped open.
6. Firmly, but gently, push the socketboard interconnect cable into the connector. Notice that the extraction tabs will move back to their locked positions when the cable is locked into the connector.
7. Repeat steps 3 through 6 to replace the waveform generator card.
8. Plug the socketboard interconnect cable into its connector on the socketboard (figure 4-2).
9. Replace the card cage by tilting it up to lock the flanges, as shown in figure 4-1, then gently setting it down. Make sure the captive fasteners line up with the fastener holes on the UniPak™ frame.
10. Tighten the captive fasteners finger tight.

4.3 TROUBLESHOOTING

This section will help you interpret and isolate failures in the UniPak™. Use it in conjunction with section 5 (Circuit Description) and the schematics provided in the back of this manual.

Three major classes of failures can occur in a system comprised of a programmer and a UniPak™. The first is no system operation, the second is poor yields, and the third is UniPak™ failure.

After successfully troubleshooting the UniPak™, you must calibrate it according to the instructions in section 4.4. It is very important that the programmer be calibrated before the UniPak™ is calibrated.

4.3.1 No System Operation

You should perform the following steps if the system will not initialize with the UniPak™ installed. After completing each step, determine whether the problem still exists.

1. Check to be sure the UniPak™ is properly installed in your programmer.
2. Check the UniPak™ programmer mating connector (J1) for bent or broken pins. (Pin HH is intentionally shorter.)
3. Check the UniPak™ cards to be sure they are correctly installed in their connectors (section 4.2).
4. Check the ribbon cable to be sure it is properly inserted in the connectors (section 4.2).
5. Check the programmer power supplies for proper voltage output levels (see programmer manual).
6. If steps 1 through 5 fail to isolate the problem, contact your local Data I/O Service Center.

4.3.2 Poor Yields

Perform the following steps if the yield rate begins to decrease. After completing each step, determine whether the problem still exists.

1. Do a complete calibration; be sure that the programmer has been calibrated first.
2. Perform waveform observations (section 4.4) for the family of the device being programmed, being careful to note any discrepancies. You may find the circuit description (section 5) and the schematics at the end of this manual useful in isolating the problem.
3. Perform calibration steps 24 and 25 on the measurement chart for the device family that is giving problems. The circuit description (section 5), schematics, and suspected components in tests 1 through 4 of table 4-1 may be helpful in isolating the problem.
4. If steps 1 through 3 fail to resolve the problem, contact your local Data I/O Service Center.

4.3.3 UniPak™ Failure

Perform the following steps if a device will not program at all or if error messages are displayed. After completing each step, determine whether the problem still exists.

1. Check that the family and pinout codes are correct for the device, and that the device is being inserted in the correct socket.
2. If possible, try a known-good device to determine whether there is a hardware problem.
3. Check to be sure the UniPak™ is properly installed.
4. Check the UniPak™ programmer mating (J1) connector for bent or broken pins. (Pin HH is intentionally shorter.)
5. Check the UniPak™ cards to be sure they are correctly installed in their connectors (section 4.2).
6. Check to be sure the ribbon cable is correctly oriented and properly inserted in the connectors.
7. Perform a complete calibration, noting any measurements falling outside the indicated limits. Refer to the corresponding test number in table 4-1 for suspected boards and components, as well as the circuit description (section 5) and the schematics, to attempt to isolate the problem.
8. Perform waveform observations and note any discrepancies. Referring to the circuit description and the schematics may be helpful in isolating the problem.
9. If steps 1 through 8 fail to resolve the problem, contact your local Data I/O Service Center.

Table 4-1. Troubleshooting Chart

TEST NUMBER	SUSPECT BOARDS	SUSPECT COMPONENTS
1	701-1998	U26, U13, CR1
2	701-1998	Q1, Q2, U14
3	701-1998	U19, U13, Q3
4	701-7997	VR1, Q23, U6, U13
5	701-7997	Q17, U8, U4, U11
	702-7995	U2, CR12
6	701-7997	Q8, U1, U4, U10, Q2, Q7, Q14, Q24, Q1
7	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
8	701-1998	U26, U13, CR1
9	701-1998	U26, U13, Q3
10	701-1998	U26
11	701-7997	U13, U14, U7, Q13, Q1, Q9
	701-1998	U18, Q4-11, U16, U17
12	701-7997	U12, U11, U4, U8, Q17
	702-7995	CR12, U2
13	701-7997	U12, U9, U4, U3, Q10
14	701-7997	U12, U10, U4, U1, Q8
15	701-1998	U25, U26, U13, CR1
16	701-1998	U25, U19, U13, CR1, Q3
17	701-7997, 701-1998	
18	702-7995	DS2, U1
19	701-7997	U1, CR8, U6, Q16, R39
20	701-7997	Q8, U1, U4, U10, Q2, Q7, Q14, Q24, Q1
21	701-7997	Q1, Q4, Q2, Q20
22	701-7997	Q1, Q18, Q21
23	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
24	701-7997	Q6, Q12, CR7, Q22
25	701-7997	U11, U4, U8, Q17
26	701-7997	U10, U4, U1, Q8
27	701-7997	Q15, U4, Q21
28	701-7997	VR2, U7
29	701-7997	U11, U4, U8, Q17
30	701-7997	U12, U10, U4, U1, Q8, CR1, CR2, U5, U2, U7, Q1, Q2, U6, Q18, CR11, Q19, Q21, Q15, Q5, U11
31	701-7997	U11, U4, U8, Q17
32-35	701-1998	RP1, RP2, U3-6
	702-7995	U9, U10, Q2
36	702-7995	DS1, U1
37	702-7995	U1, CR8
38	701-1998	U1, U2, U12, Q12-19
39	701-1998	U1, U2, U12, Q12-19
40	701-1998	U1, U2, U12, Q12-19
41	701-1998	U1, U2, U12, Q12-19
42	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
43	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
44	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
45	701-7997	Q10, U3, U4, U9, Q1, Q13
	701-1998	U18, Q4-11, U16, U17
46	702-7995	DS3, U1
47	702-7995	U2, CR14
48	702-7995	DS4, U1
49	702-7995	U2, CR15
50	702-7995	DS5, U1
51	702-7995	U2, CR11
52	702-7995	DS6, U1
53	702-7995	U2, CR13
54	702-7995	DS7, U1
55	702-7995	U2, CR16
56	702-7995	Q1, RP1, U3, CR17

4.4 CALIBRATION

The need for calibration varies with the amount of use your UniPak™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums, or 2) troubleshooting has been completed, or 3) the user's company policy requires periodic calibration certification.

NOTE

If calibration or repair is required but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center.

Because of differences in programmer mainframes, this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the UniPak™.

Calibration of the UniPak™ consists of three parts:

1. Power Supply Calibration—measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC Calibration—consists of measuring and adjusting critical DC voltage levels generated by the UniPak™.
3. Waveform Observation—enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

The first part of the calibration procedure (power supply calibration) varies with the type of programmer you have. Therefore, this manual refers you to your programmer manual for details on power supply calibration.

DC calibration is discussed in section 4.4.1, the optional verify voltage checks are described in 4.4.2, and waveform observation is detailed in section 4.4.3. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the UniPak™:

- Data I/O calibration extender (part number 910-1521)
- Three and a half-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

Check the appropriate programmer manual for any additional equipment that you may need to calibrate the programmer.

To prepare your UniPak™ for calibration, follow the procedures outlined below:

1. Turn the programmer power off; see section 3.3 for details.
2. Remove the UniPak™ from the programmer; see section 2.3 for details.
3. Insert the calibration extender into the programmer the same way you insert the UniPak™ (section 2.2).
4. Unscrew the two thumb screws (captive fasteners) located on the underside of the top cover of the UniPak™ (figure 4-1); they connect the card cage to the socket assembly. Separate the two parts of the assembly.

CAUTION

Do not let the fasteners short to the motherboard.

5. Insert the 64-pin connector of the card cage into the mating connector on the calibration extender (figure 4-5, detail B).
6. Lean the top portion of the UniPak™ against its bottom portion at a 45-degree angle (see figure 4-5).

NOTE

Be sure the socket assembly flange locks into the card cage flange (see figure 4-5, detail A).

Do not allow the frame of the socket assembly to short to the memory board.

Be careful not to strain the cable or scratch the top of the programmer.

4.4.1 DC Calibration

The DC calibration procedure described in this section enables you to adjust critical DC voltage levels generated by the UniPak™. To follow this procedure, use the measurement chart at the end of this section. This measurement chart contains the information needed for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.—tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.—identifies individual tests.
- Test Description—identifies the functions being tested.
- Measurement Test Location—tells which socket pins, circuit boards, or test points to probe for measuring voltages.
- Measurement—specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the UniPak™ until the problem is corrected.
- Adjustment Location—tells which potentiometer to adjust if a measurement is out of range.
- Comments—gives special instructions for particular tests.

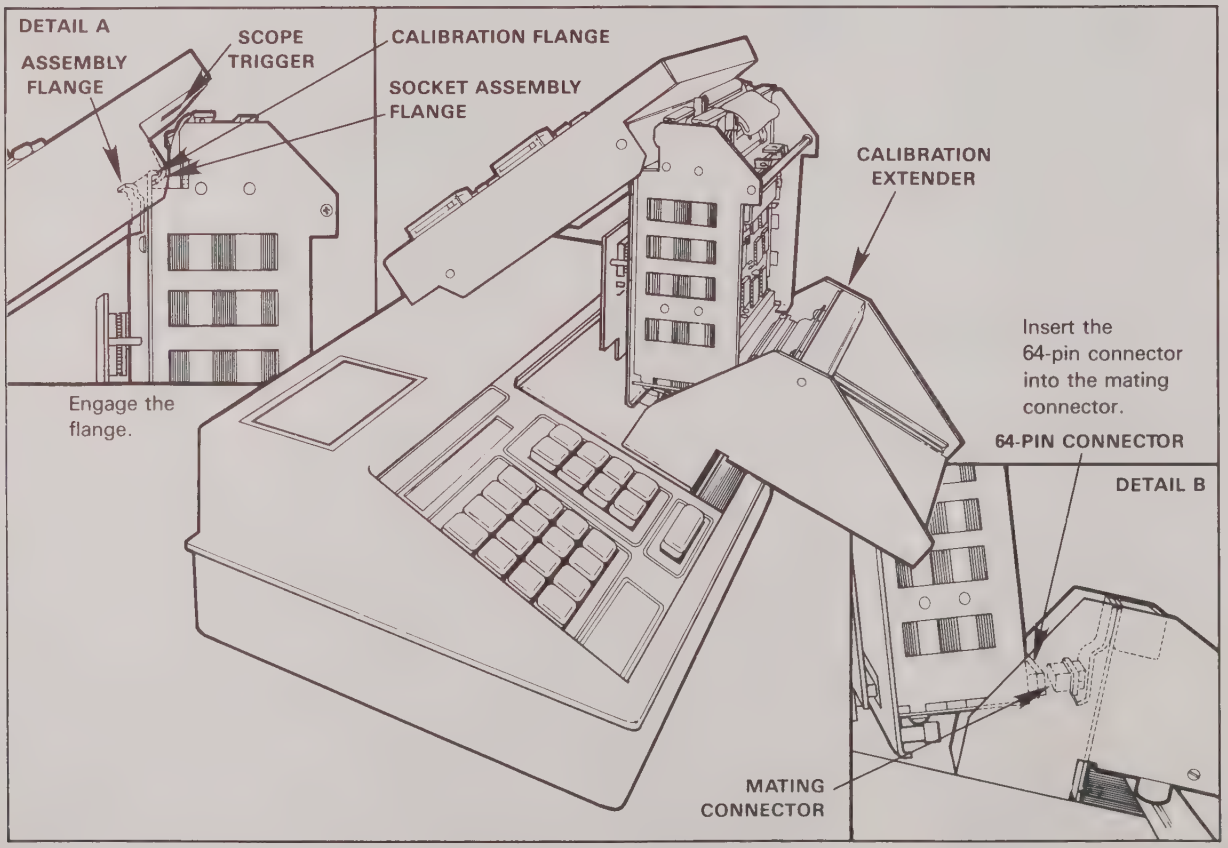


Figure 4-5. Calibration Setup

The DC calibration procedure is as follows:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.8 for details). Waveform generation may damage any device in the UniPak™ sockets.

1. Turn the programmer power on (section 3.2).
2. Put the programmer into the calibration mode by following the key sequences in table 4-2.
3. Perform the general calibration steps (steps 1 through 20) on the measurement chart. For steps 4 and 5, refer to the figures at the end of the measurement chart to observe the bit switch rise waveform and the DAC step waveforms.

Table 4-2. Key Sequence To Access the Calibration Mode

Programmer System	Key Sequence To Enter Calibration Mode	To Increment Step No.	To Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number* Press START	Press ENTER	Press REVIEW
29A/ 29B	Press SELECT Press C1 Press START Enter Step Number* Press START	Press START	Press REVIEW
100A	Press SELECT Press 12 Enter Step Number* Press START	Press START	Press BACK-SPACE

*Optional

For each general calibration step on the measurement chart do the following:

- Take measurement readings at the device sockets or test points indicated on the measurement chart; figure 4-6 shows the pin numbers for the sockets; figure 4-7 shows test points.
- Ground the digital voltmeter to socket 7, pin 10 on the front panel of UniPak™.

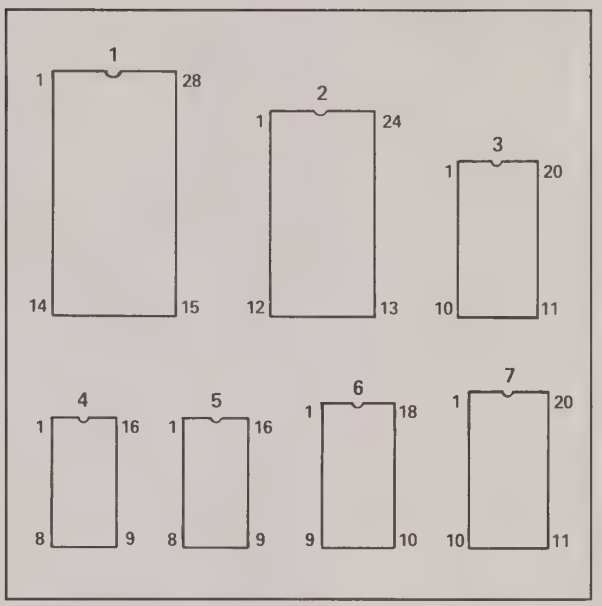


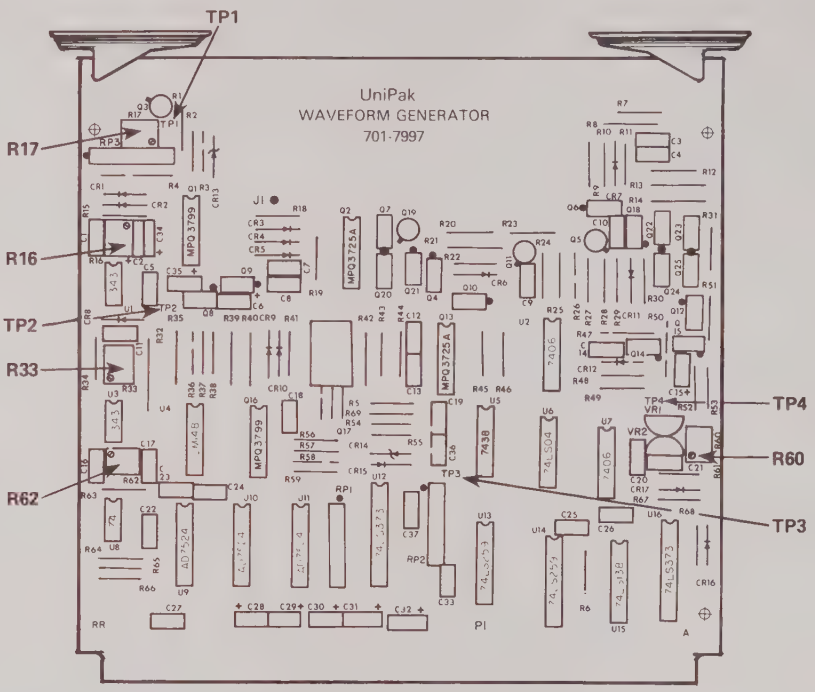
Figure 4-6. Pin Numbers of Device Sockets

- The adjustment pots on the waveform generator, memory board, and the address card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-7 shows the location of these adjustment points.
- Access each new step by pressing the START (or ENTER) key. The new step number will appear in the display when the UniPak™ is ready for the next step. To go back to a previous test, press the REVIEW (or BACKSPACE) key.

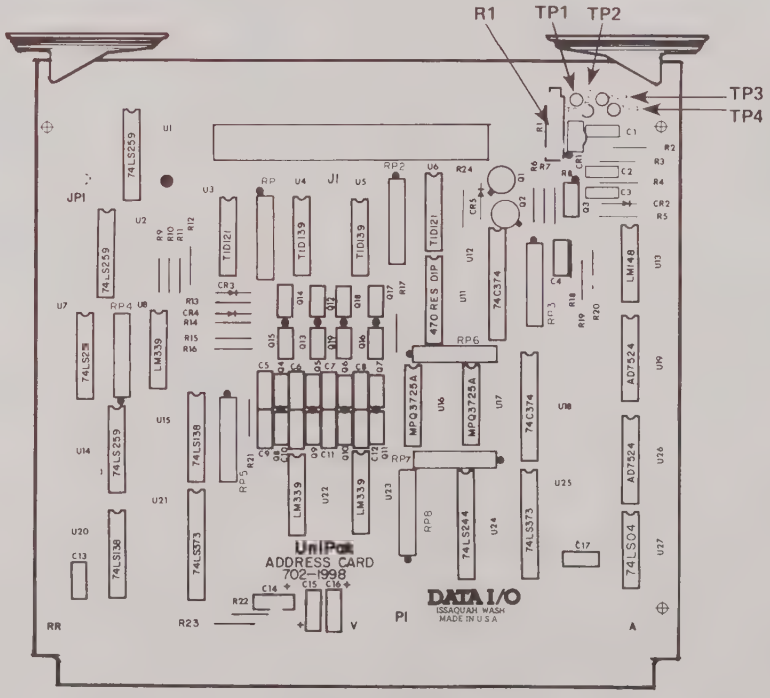
NOTE

The remaining steps on the measurement chart (steps 24 through 28) are family specific. These steps are optional and have been included for your convenience.

4. For each family-specific calibration step on the measurement chart, do the following to enter the family and pinout codes:
   - Perform a **load operation**; refer to your programmer manual for details.
   - Enter the family and pinout codes when prompted by the programmer; refer to your programmer manual for further information.
   - Fill RAM with data specified on the timing diagram.
   - Put the programmer back into the calibration mode; see figures 4-8, 4-9, and 4-10 for the key sequence.
   - Enter the step number from the measurement chart.
   - Press START.



a. Waveform Generator, 701-7997



b. Address Card, 702-1998

Figure 4-7. Adjustment Locations

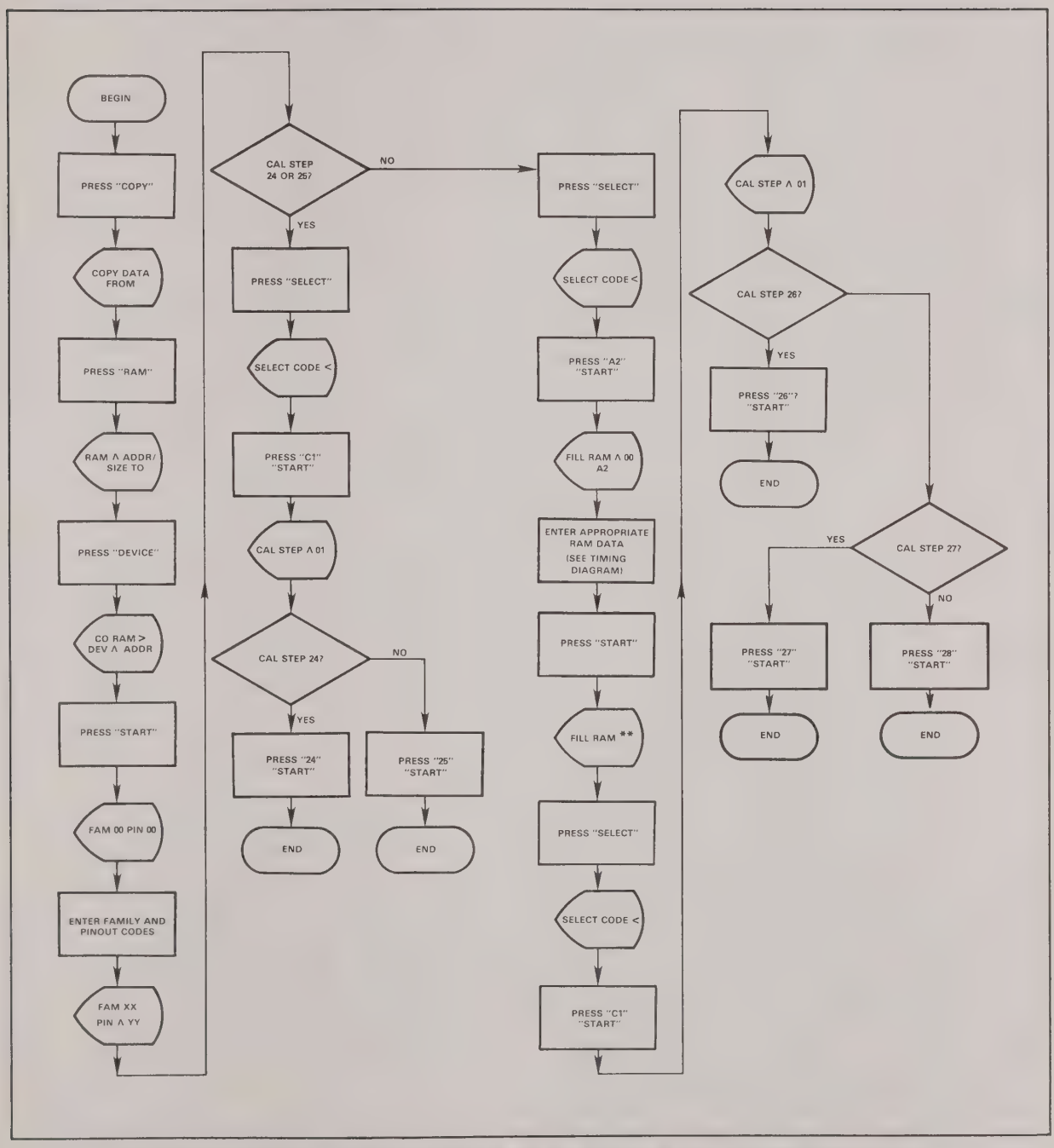


Figure 4-8. Accessing Calibration Steps 24, 25, 26, 27, and 28 (29A Universal Programmer)

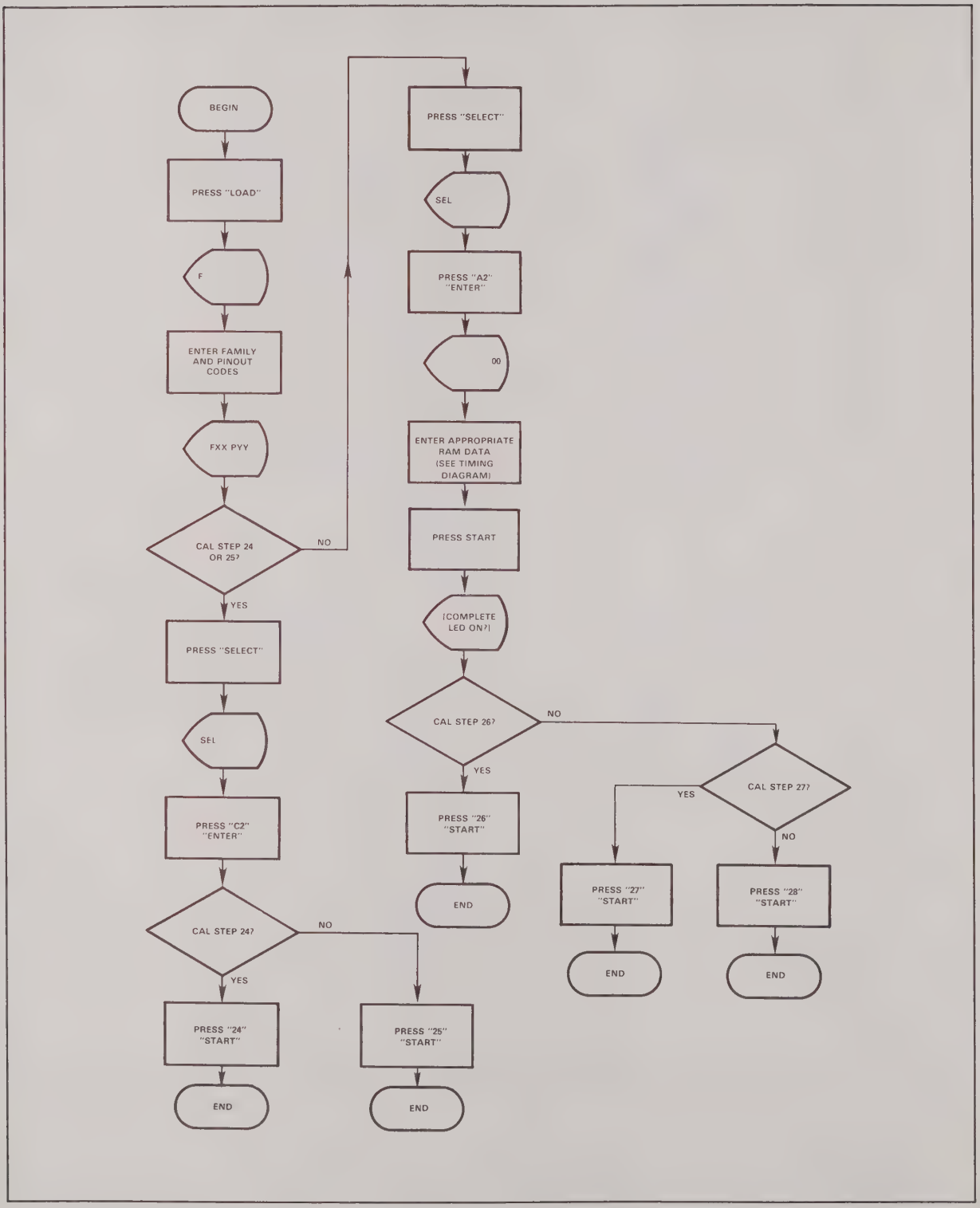


Figure 4-9. Accessing Calibration Steps 24, 25, 26, 27, and 28 (System 19)

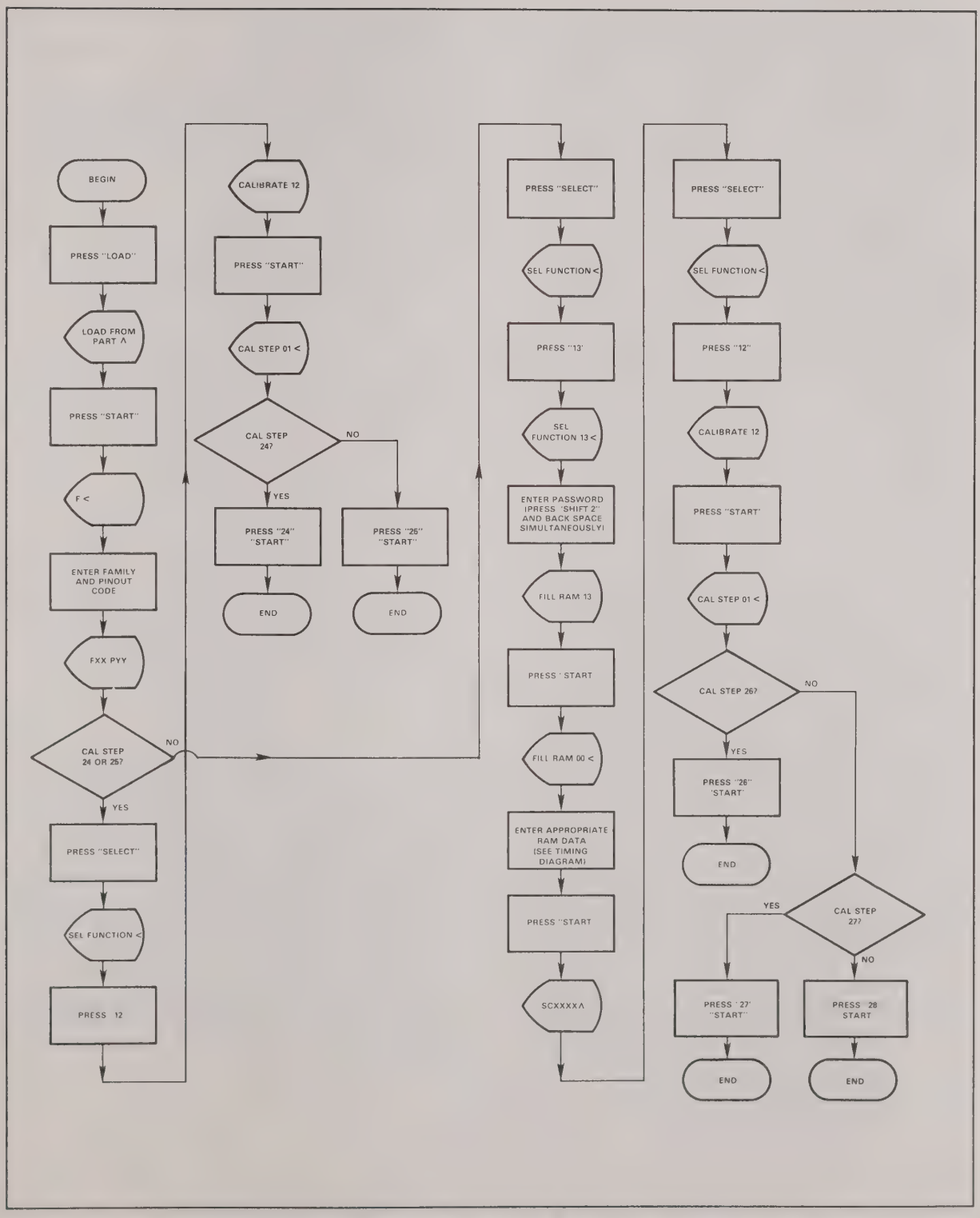


Figure 4-10. Accessing Calibration Steps 24, 25, 26, 27, and 28 (Model 100A)

4.4.2 Optional Verify-Voltage Checks

Two calibration steps (24 and 25) have been provided for the measurement of first- and second-pass verify voltages. The family characteristics table in the applicable family timing diagram defines the levels for first- and second-pass verifications for each family. These are provided for the investigation of yield problems; no adjustments are available. Under normal circumstances, these steps can be eliminated from a routine calibration.

4.4.3 Waveform Observation

Programming waveforms of your UniPak™ can be observed with an oscilloscope and compared with the timing diagrams that are provided in appendix B. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the UniPak™ is performing to the device manufacturer's specifications. Since the UniPak™ generates a large number of waveforms and all calibration adjustments are accomplished in DC calibration, it is necessary only to observe waveforms for commonly used devices or those that are presenting yield problems.

During the waveform observation phase of the calibration procedure, your UniPak™ uses a firmware routine that generates programming waveforms for the data stored in system RAM. An oscilloscope trigger pulse is generated for every address increment. This occurs after the reject pulse count has been reached for all the bits being programmed in the previous data word. The address is automatically reset to Ø when the maximum PROM address is reached, and incrementing continues. Waveform observation can be done with the UniPak™ either on the calibration extender or plugged into the programmer.

The waveform observation procedure described below calls for filling RAM with data so that it is possible to observe bit-to-program waveforms. The procedure takes into account the device type (VOL or VOH) so that for either type of PROM, a bit-to-program will appear on the same socket contact.

When used with a timing diagram, this procedure allows you to compare waveforms on the oscilloscope with the waveform photographs on the timing diagram for any type of device; a detailed explanation of the timing diagrams is provided in section 4.4.4. The waveform observation procedure is as follows:

1. Refer to table A-1 to determine the family and pinout codes, polarity, and technology of the selected device.

NOTE

Polarity is indicated in the family code. Odd-numbered families are VOL and even-numbered families are VOH.

2. Initiate a load operation; refer to section 3.4 for details.
3. Key in the family and pinout codes when prompted by the programmer; see section 3.5.
4. Fill your programmer's RAM with programming data listed in the timing diagram for the family code entered: The correct data depends on the polarity and technology of the device. Refer to table 4-3 for the "Fill RAM" key sequence.

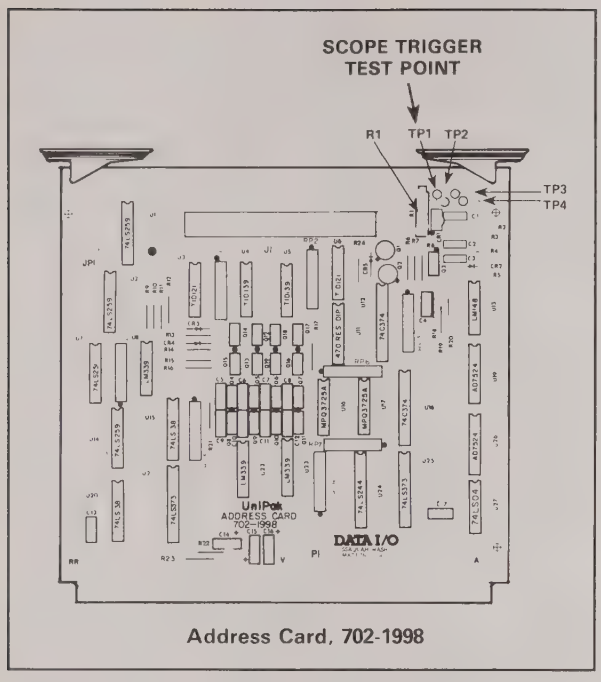
CAUTION

Remove all devices before entering the calibration mode. Waveform generation may damage any device in the UniPak™ sockets.

Table 4-3. Key Sequence To Fill RAM With Data

System	Key Sequence
19	Press SELECT A 2 Press ENTER Enter data Press START
29A/29B	Press SELECT A 2 Press START Enter data Press START
100A	Press SELECT 1 3 Enter Password (SHIFT 2/ BACKSPACE Enter data Press START

5. Enter the waveform generation mode at step 26 on the measurement chart by following the key sequences listed in figure 4-8.
6. Erase waveforms for EEPROMs are observable at steps 27 and 28 of the measurement chart by following the key sequences listed in figure 4-8, 4-9 or 4-10, depending on your programmer.
7. Trigger your oscilloscope by connecting to the test point under the top of the address card (see figure 4-11).
8. Ground the scope to the GND contact of the socket with its LED illuminated; the GND contacts are shown in figure 4-12.



Address Card, 702-1998

Figure 4-11. UniPak™ Scope Trigger Test Point

9. To observe individual waveforms, refer to figure 4-12 under the pinout code number entered in step 3. The individual socket illustrations give the numbers of the socket contacts to probe when observing the waveforms on the timing diagram.

NOTE

Considerations helpful in setting up and interpreting the waveform displays are explained in section 4.4.4.

4.4.4 Detailed Explanation of the Timing Diagrams

This manual contains a timing diagram for each device family that can be programmed by the UniPak™. Each timing diagram contains a set of waveform photographs that show critical programming parameters. To use these diagrams and photographs, read the information provided below and refer to the sample timing diagram (figure 4-13).

1. FAMILY CODE NUMBER--corresponds to the family code number of the device (refer to table A-1).
2. FAMILY CHARACTERISTICS TABLE—lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered noncritical with a ±10% tolerance.
3. NOTES—important information pertaining to a timing diagram.
4. WAVEFORM NAMES—correspond to the pin names on the pinout chart (figure 4-12); the pinout chart tells you which socket pins to probe when you are observing the waveforms for a particular device pinout within a family. (The pinout is indicated by the number above each socket in figure 4-12 which corresponds to the pinout code in table A-1.)

We recommend that you use the oscilloscope's single-sweep mode for address observation, since one trigger pulse is generated for each address change.

- BIT NO PROG—Always use the 02 (bit 2) contact (shown in figure 4-12).
- BIT TO PROG—Always use the 01 (bit 1) contact (shown in figure 4-12).

5. LAYOUT SEQUENCE NUMBER—used as a reference point within each diagram.
6. DELAY TIME POSITION—indicates the time from the start of the main sweep to the start of the delay time.
7. OSCILLOSCOPE GROUND REFERENCE—ground contact on the socket with its LED illuminated.
8. TIME-BASE AND VOLTS-PER-DIVISION SETTINGS—Horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By taking into account any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.
9. EXPANDED PHOTOGRAPH NUMBER—corresponds to the photograph number. These detailed photographs are included to magnify rapid voltage changes or particular pulses in a pulse train.
10. VOLTAGE—indicates volts per division. The one in the upper left corner is for the top trace, and that in the lower left corner is for the bottom trace.

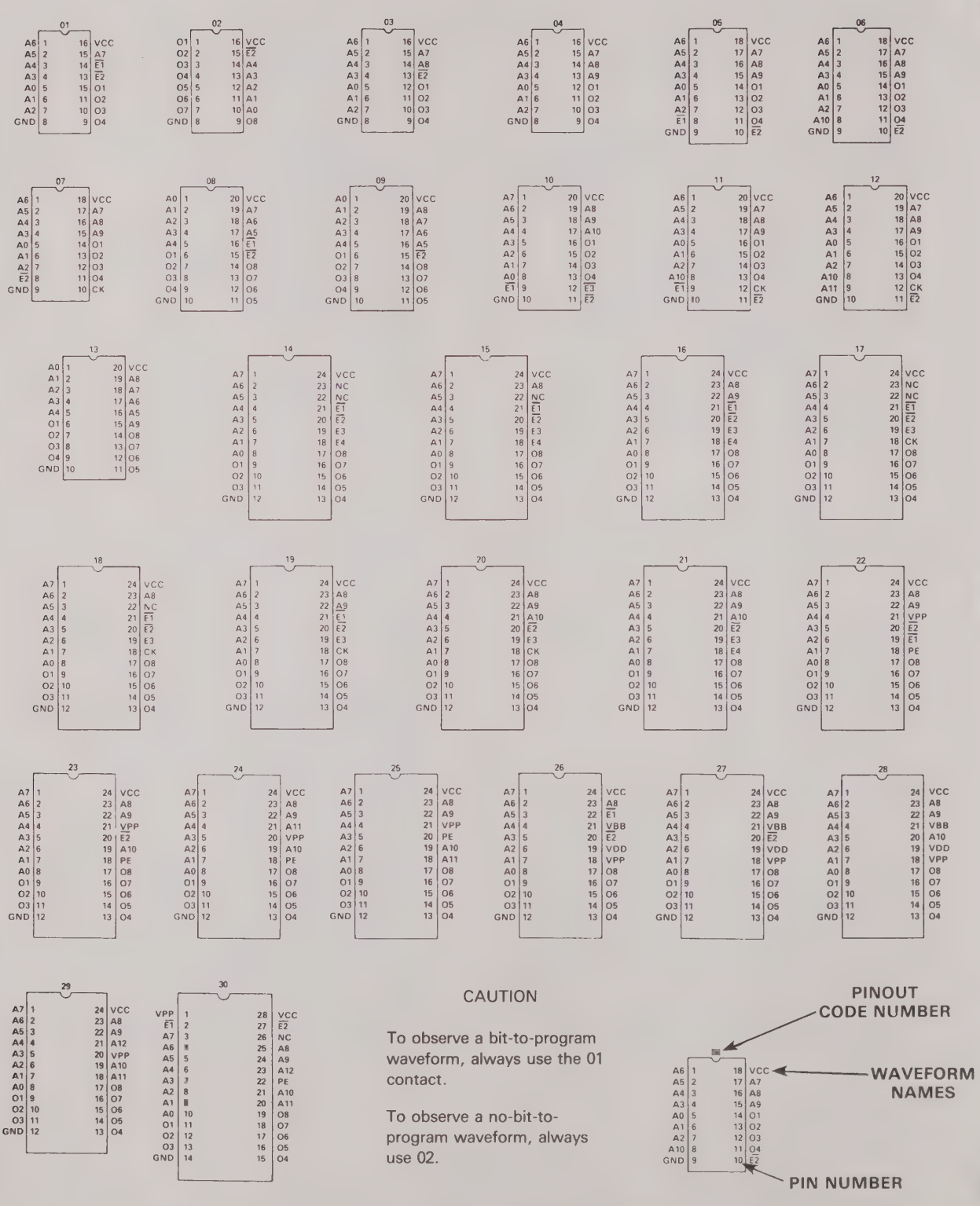


Figure 4-12. Pin Names by Pinout Code Numbers

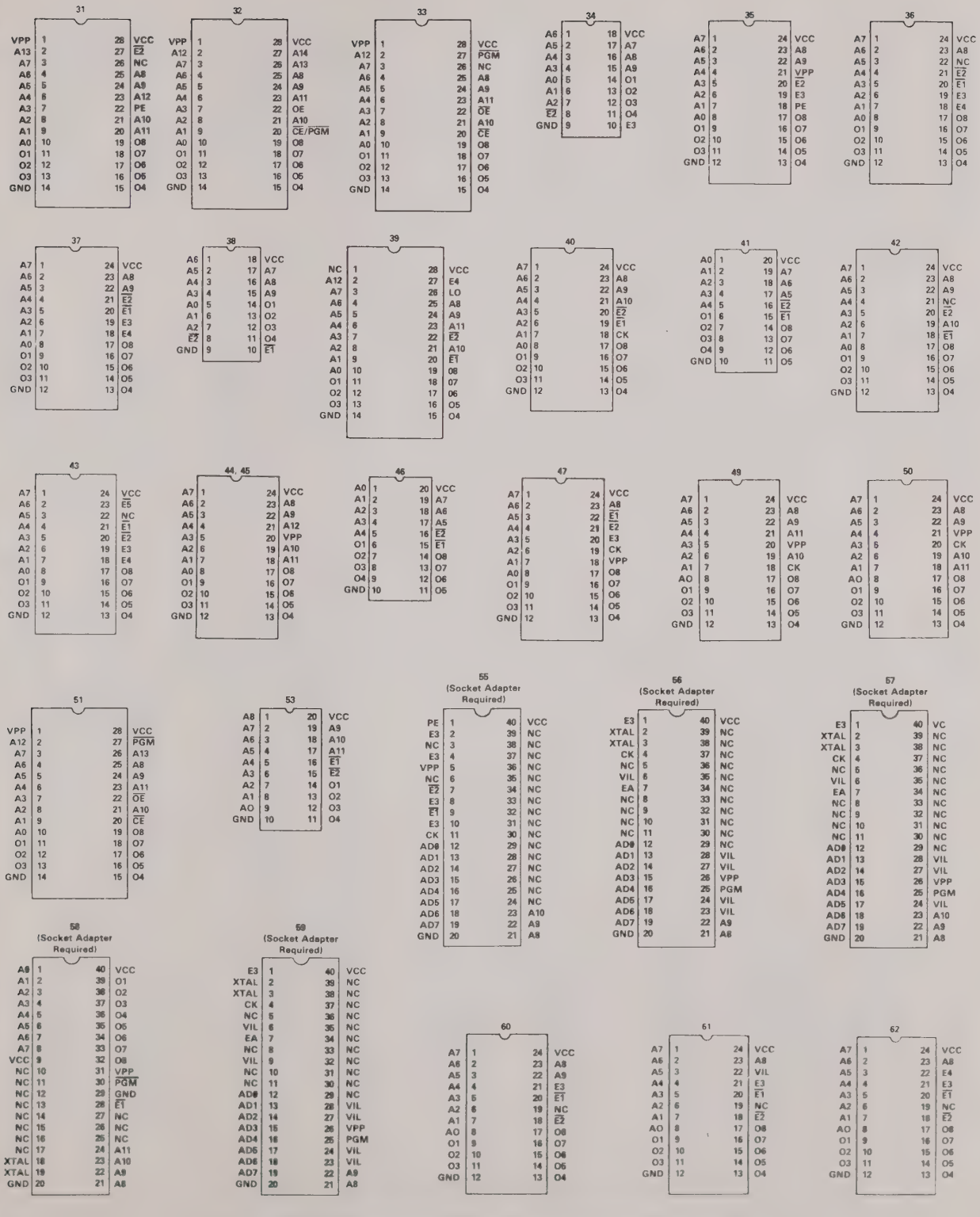


Figure 4-12. Pin Names by Pinout Code Numbers (Continued)

Figure 4-12. Pin Names by Pinout Code Numbers (Continued)

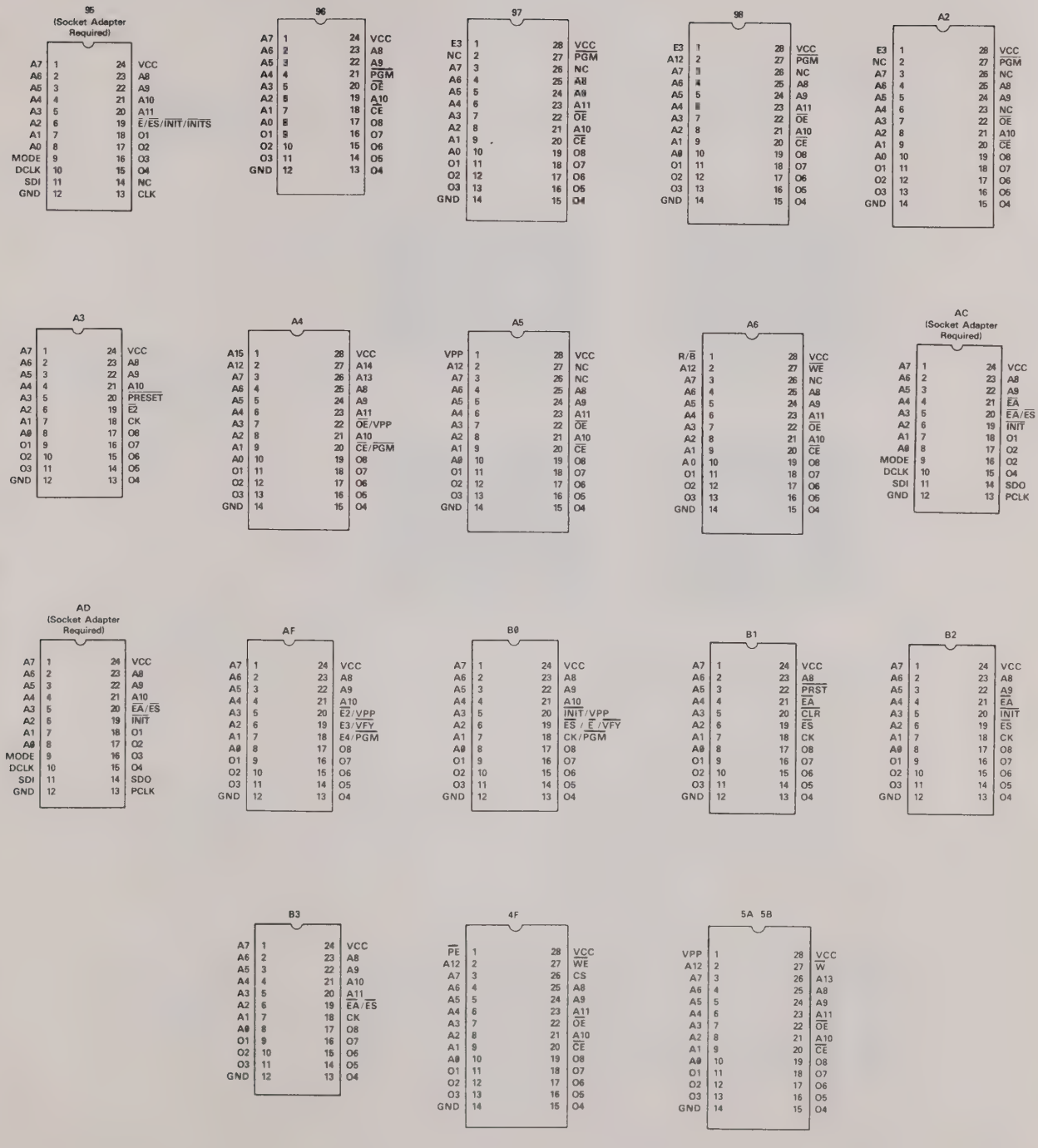


Figure 4-12. Pin Names by Pinout Code Numbers (Continued)

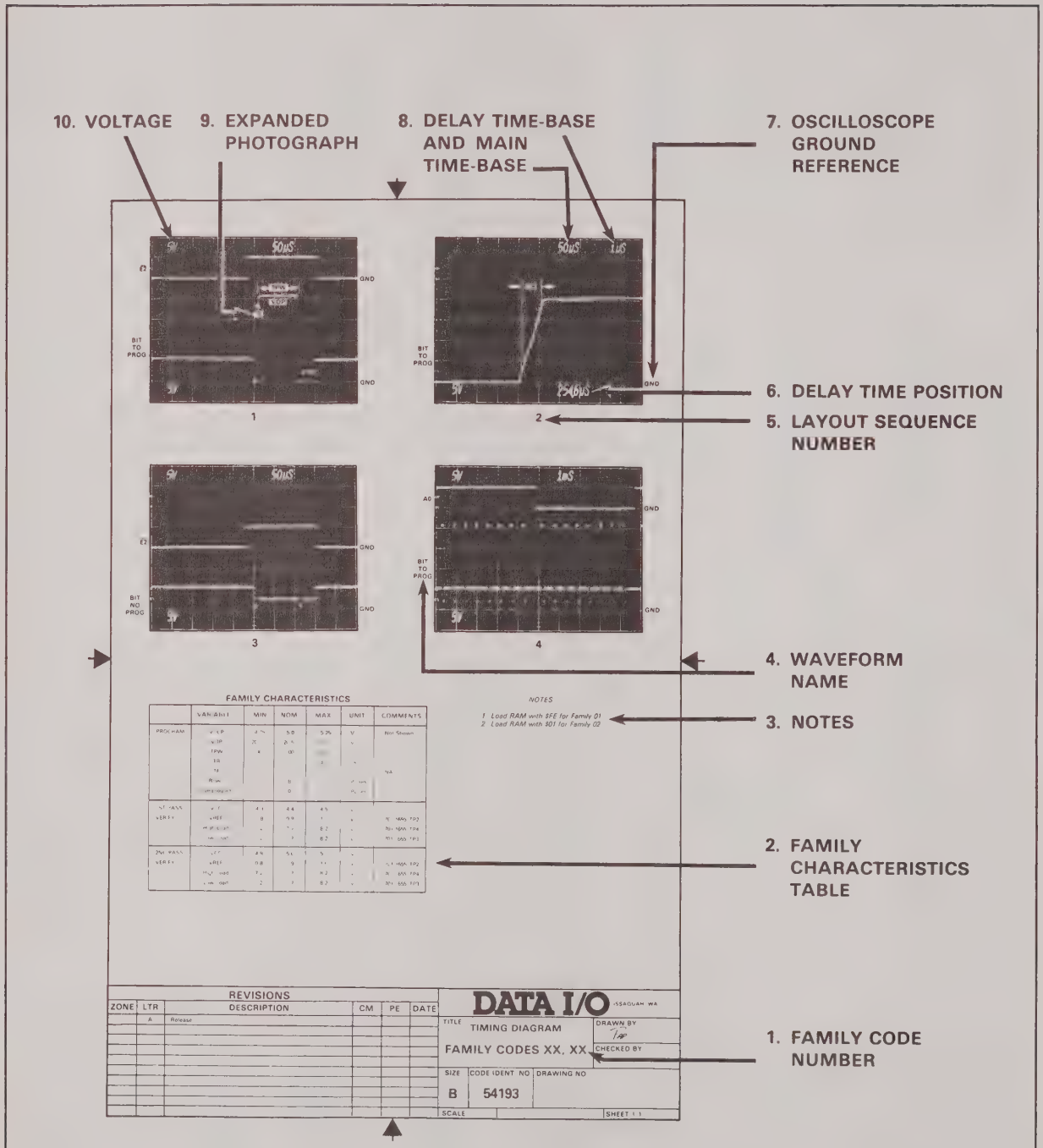


Figure 4-13. Sample Timing Diagram

Measurement Chart

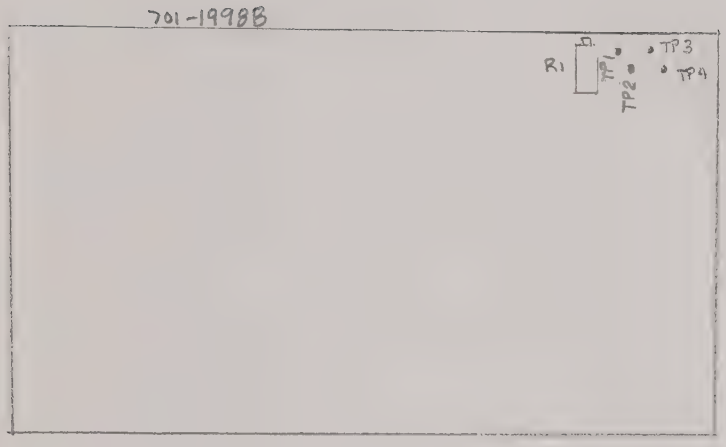


Table 4-4. Measurement Chart

REVISIONS

LTR	DESCRIPTION	P.E	DATE
D	ECN 5022		2/84

UniPak^{tm} Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
			The following tests are performed					
			with the UniPak™ on the calibration					
			extender:					
			Socket/Pin					
1	1	V reference supply	701-1998/TP4	10.20V	10.24V	10.28V	R1,701-1998	
	2	Load supply (high range)	701-1998/TP2	24.3V		25.7V		
	3	Load supply (low range)	701-1998/TP3	24.3V		25.7V		
	4	Supply reference	701-7997/TP4	4.98V	5.00V	5.02V	R60, 701-7997	
	5	V_{CC} supply	2 24	11.9V	12.0V	12.1V	R62,701-7997	
	6	CE supply	2 20	32.7V	33.0V	33.2V	R16,701-7997	
	7	Bit supply	2 9	25.7V	26.0V	26.2V	R33,701-7997	
2	8	V reference supply	701-1998/TP4	6.70V		6.90V		
	9	Load supply	701-1998/TP3	10.3V		11.7V		
3	10	V reference supply	701-1998/TP4	3.30V		3.50V		

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
D	ECN 5022		2/84

UniPak™ Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
4	11	Bit switch rise waveform	2 14				R17, 701-7997	See waveform photograph (page 4-27)
5		DAC step waveforms						
	12	V_{CC}	2 24					See waveform photograph (page 4-28)
	13	Bit supply	701-7997/TP2					See waveform photograph (page 4-29)
	14	CE supply	701-7997/TP1					See waveform photograph (page 4-28)
	15	V_{REF} supply	701-1998/TP4					See waveform photograph (page 4-29)
	16	Load supply	701-1998/TP3					See waveform photograph (page 4-26)
			The following tests are performed					
			with the UniPak™ installed in its					
			normal operating position.					
6	17	All voltages off	all all	-0.1V		0.4V		
7	18	Socket 2 LED						Confirm that socket 2 LED is on
	19	V_{CC} supply load	2 24	11.8V		12.1V		Place a 20-ohm, 2W resistor
								between pins 24 and 12, socket 2

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
D	ECN 5022		2784

UniPak^{tm} Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
8	20	CE supply load	2 20	32.3V		33.2V		Place a 100-ohm, 10W resistor
								between pins 20 and 12,socket 2.
	21	Pin 18 voltage switch	2 18	32.7V		33.2V		
	22	Pin 21 voltage switch	2 21	32.7V		33.2V		
9	23	Bit supply load	2 11	25.2V		26.0V		Place a 100-ohm, 5W resistor
								between pins 11 and 12,socket 2.
	24	Pin 19 voltage switch	2 19	24.9V		25.5V		
10	25	V_{CC} voltage linearity	2 24	3.90V		4.10V		
	26	CE supply linearity	2 18	23.0V		23.5V		Place a 2.2K-ohm, 1/2W resistor
								between pins 12 and 18,
								socket 2.
	27	-5V supply	2 21	-5.2V		-4.8V		
	28	12V supply	2 20	11.4V		12.6V		
11	29	V_{CC} voltage linearity	2 24	4.90V		5.10V		

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
D	ECN 5022		2/84

UniPak[tm] Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
	30	CE supply linearity	2 21	11.4V		12.0V		
12	31	V_{CC} voltage linearity	2 24	5.90V		6.10V		
	32	I source and pulldowns	2 9,11,14,16	2.0V		2.6V		
	33	I source and pulldowns	2 10,13,15,17	0.0V		1.0V		
13	34	I source and pulldowns	2 10,13,15,17	2.0V		2.6V		
	35	I source and pulldowns	2 9, 11, 14, 16	0.0V		1.0V		
14	36	Socket 1 LED						Confirm that socket 1 LED is on.
	37	V_{CC} voltage supply	1 28	4.90V		5.10V		
	38	Odd address and data	1 2,3,5,7,9,11,13,16,18,	3.0V		6.0V		
		high	20,22,24,26					
	39	Even address and data	1 1,4,6,8,10,12,15,17,19,21,	-0.1V		0.4V		
		low	23,25,27					
15	40	Odd address and data	1 2,3,5,7,9,11,13,16,18,	-0.1V		0.4V		
		low	20,22,24,26					
	41	Even address and data	1 1,4,6,8,10,12,15,17,19,21,	3.0V		6.0V		
		high	23,25,27					
16	42	Odd data lines high	1 11,13,16,18	25.5V		26.5V		
	43	Even data lines pullups	1 12,15,17,19	4.5V		5.5V		

* DO NOT USE FLUKE 8506A DVM FOR THESE READINGS
IMPEDANCE AFFECTS READINGS.

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
D	ECN 5022		2/84

UniPak^{tm} Measurement Chart

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/Pin	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
17	44	Odd data lines pullups	1 11,13,16,18	4.5V		5.5V		
	45	Even data lines high	1 12,15,17,19	25.5V		26.5V		
18	46	Socket 3 LED						Confirm that socket 3 LED is on.
	47	V_{cc} voltage supply	3 20	4.90V		5.10V		
19	48	Socket 4 LED						Confirm that socket 4 LED is on.
	49	V_{cc} voltage supply	4 16	4.90V		5.10V		
20	50	Socket 5 LED						Confirm that socket 5 LED is on.
	51	V_{cc} voltage supply	5 16	4.90V		5.10V		
21	52	Socket 6 LED						Confirm that socket 6 LED is on.
	53	V_{cc} voltage supply	6 18	4.90V		5.10V		
22	54	Socket 7 LED						Confirm that socket 7 LED is on.
	55	V_{cc} voltage supply	7 20	4.90V		5.10V		
23	56	V_{cc} pullup 1 on	1 28	4.0V		5.2V		
		V_{cc} pullup 2 on	2 24	4.0V		5.2V		
		V_{cc} pullup 3 on	3 20	4.0V		5.2V		
		V_{cc} pullup 4 on	4 16	4.0V		5.2V		
		V_{cc} pullup 5 on	5 16	4.0V		5.2V		
		V_{cc} pullup 6 on	6 18	4.0V		5.2V		
		V_{cc} pullup 7 on	7 20	4.0V		5.2V		

Table 4-4. Measurement Chart (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
D	ECN 5022		2/84

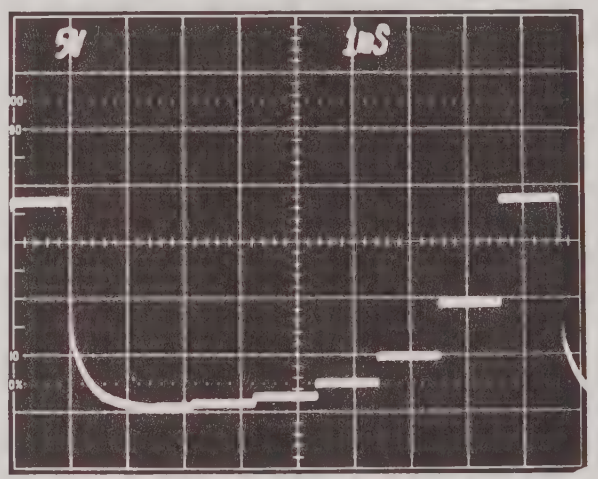
UniPak^{tm} Measurement Chart

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground DMM to socket 7, pin 10
			Steps 24 through 28 are optional.					
24	57	Static 1st-pass verify						See family characteristics table
		levels						in the applicable timing
								diagram.
25	58	Static 2nd-pass verify						See applicable timing diagram.
		levels						
26	59	Programming waveforms						See applicable timing diagram.
27	60	Chip-erase waveforms						See applicable timing diagram.
								For electrically erasable
								devices only.
28	61	Byte-erase waveforms						See applicable timing diagram.
								For electrically erasable
								devices only.

Measurement Chart

PROGRAM ELECTRONICS _____

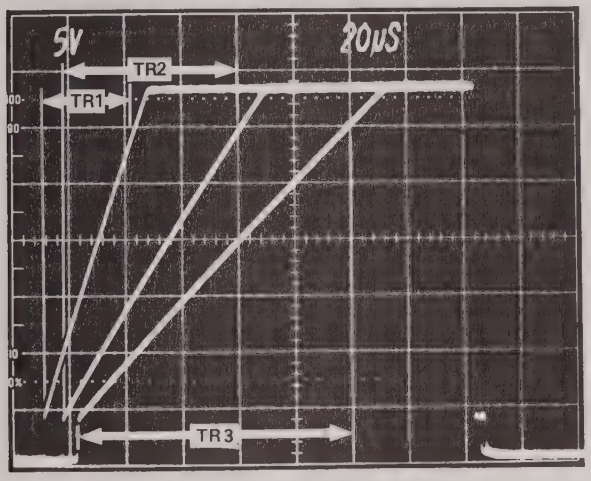
DAC Step Waveform



DAC Load Supply

DATE	REV	REVISION RECORD	DR	CK
3/84				

Bit Switch Rise-Time Waveform



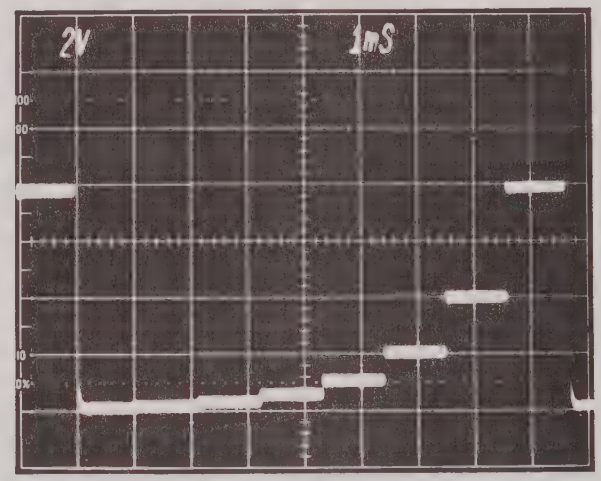
	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	TR1	26	33	37	µs	
	TR2	62	66	70	µs	Adjust R17, 701-7997.
	TR3	90	100	110	µs	

NOTE: All TR's are measured from 10% to 90%.

Measurement Chart

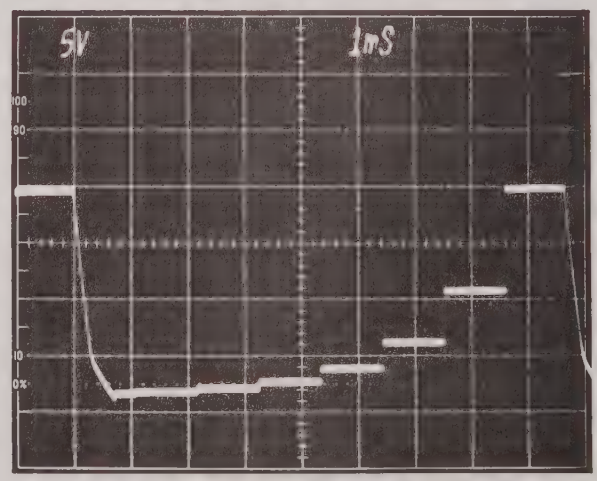
PROGRAM ELECTRONICS _____

DAC Step Waveform



V_{CC} DAC

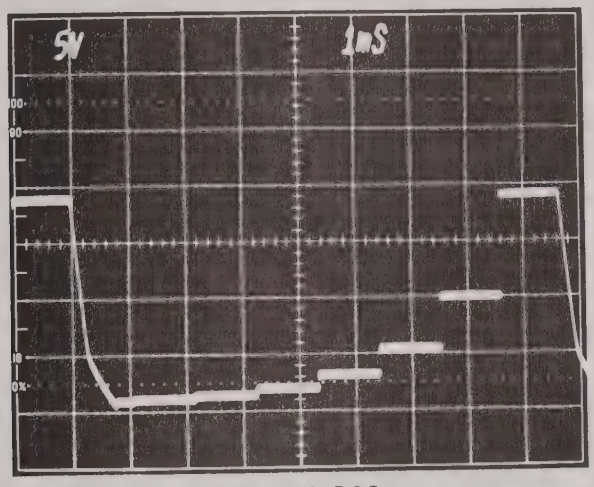
DAC Step Waveform



$\overline{CE}$ Supply DAC

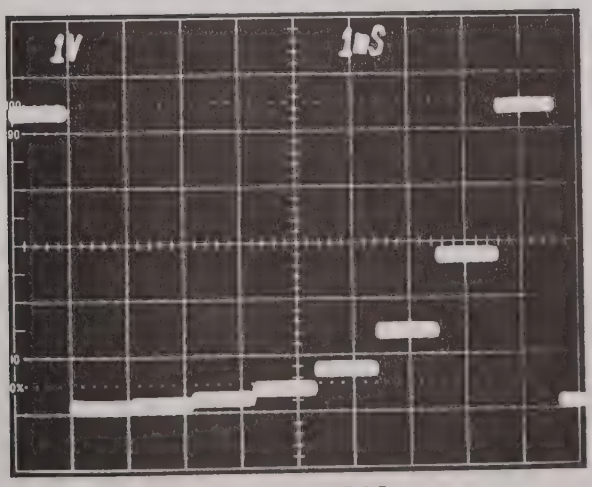
DATE	REV	REVISION RECORD	DR	CK
3/84				

DAC Step Waveform



Bit Supply DAC

DAC Step Waveform



V_{REF} Supply DAC

SECTION 5
CIRCUIT DESCRIPTION

5.1 OVERVIEW

This section defines the functions of UniPak™ principal hardware components. Each circuit-card assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

5.2.1 The Link Between the UniPak™ and the Programmer

The UniPak™ is controlled by the programmer's extended processor bus (J6), through the UniPak™'s mating connector. Pin functions of the extended processor bus are shown in table 5-1.

The control software for the UniPak™ is located in EPROM on the memory card (702-0045).

5.2.2 The Buses

The programmer's address bus, data bus, R/$\overline{W}$ line and $\overline{V \bullet \emptyset_2}$ line access the software on the memory card and control the gates and registers on the waveform generator (701-7997) and address and data driver cards (701-1998). The UniPak™'s device bus gathers the programming waveforms produced by these cards and transmits them to the socket card (702-7995). Figure 5-1 shows the relationships between the buses.

Table 5-1. Pin Functions, Programmer's Extended Processor Bus (at J1-J3)

Pin	Function	Pin	Function
1	A_0	A	A_5
2	A_1	B	A_6
3	A_2	C	A_7
4	A_3	D	A_8
5	A_4	E	A_9
6	A_{10}	F	A_{11}
7	A_{12}	H	A_{13}
8	A_{14}	J	A_{15}
9	DO_1	K	DI_1
10	DO_2	L	DI_2
11	DO_3	M	DI_3
12	DO_4	N	DI_4
13	DO_5	P	DI_5
14	DO_6	R	DI_6
15	DO_7	S	DI_7
16	DO_8	T	DI_8
17	Ver. A	U	Ver. B
18	Start	V	Clk. Inh.
19	W/L	W	"26"
20	VOL/VOH	X	"36"
21	+5V	Y	−9V
22	+Prog.	Z	+24V
23	GND	AA	−5V
24	Sense	BB	Operate
25	+48V	CC	Unreg. H.V.
26	GND	DD	Gnd.
27	C1	EE	C4
28	C2	FF	C5
29	C3	HH	C6
30	IRQ	JJ	Gate Enable
31	R/W	KK	Extend
32	V•Ø2	LL	+18V Raw
33	Interlock	MM	PP
34	+10V Raw	NN	RR
35	Write	PP	Read
36	Reset	RR	Fwd.

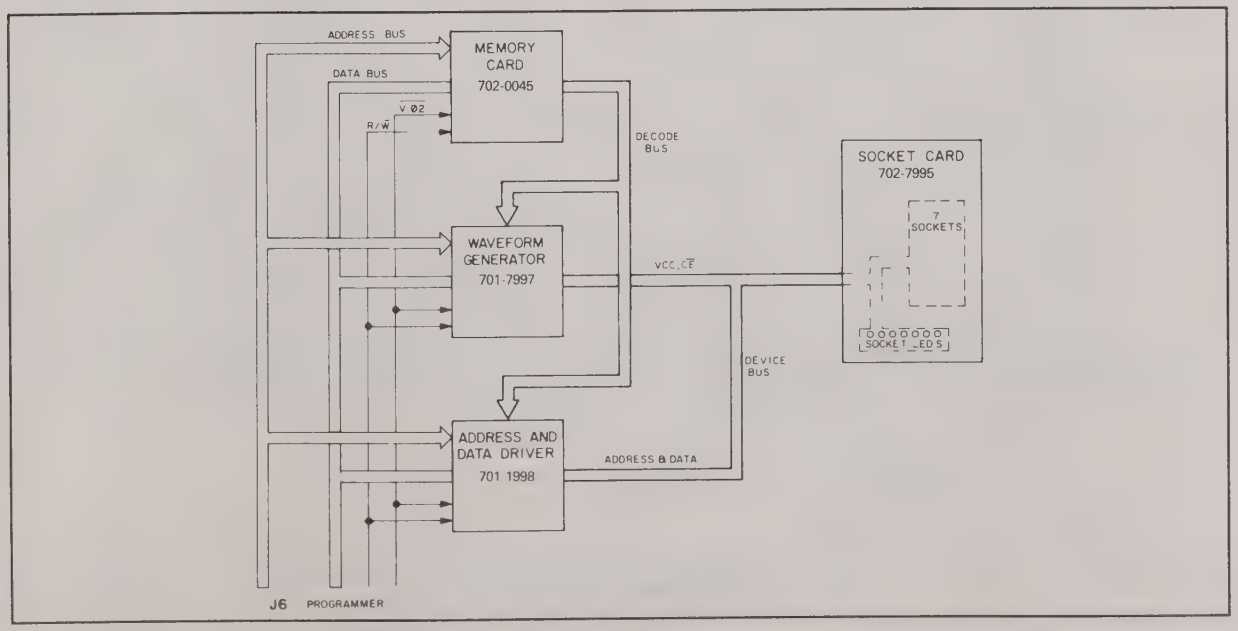


Figure 5-1. Block Diagram, UniPak™ Electronics

5.3 COMPONENT LAYOUT

Figure 5-2 shows the component layout of the UniPak™. The principal components are described in paragraphs 5.3.1 through 5.3.5.

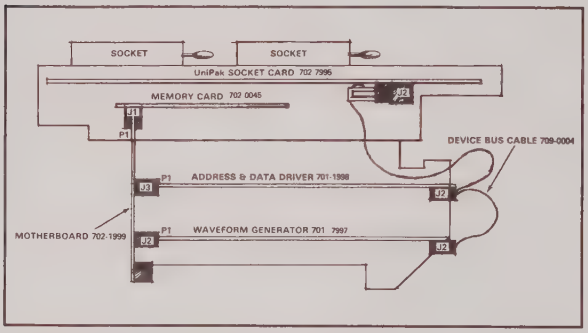


Figure 5-2. Principal Components of the UniPak™

5.3.1 Motherboard

The motherboard accepts the signals and power supplies from the J6 of the programmer and transmits them to two identical 72-pin edge connectors and a 50-pin edge connector (see figure 5-3 and schematic 008-1999).

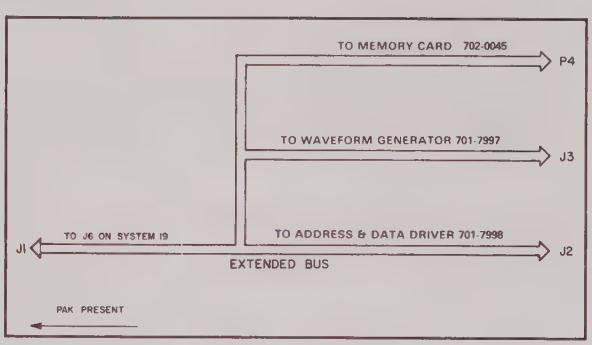


Figure 5-3. Block Diagram, UniPak™Motherboard

5.3.2 Waveform Generator

The waveform generator provides all signals, including addresses and data, required for programming devices. These signals are generated by the blocks shown in figure 5-4.

Three major supplies are the V_{CC} supply, the CE supply and the bit supply, which are used to generate the respective signals. Each supply is software-controlled via a D/A converter. All DACs obtain their reference voltage from the DAC reference.

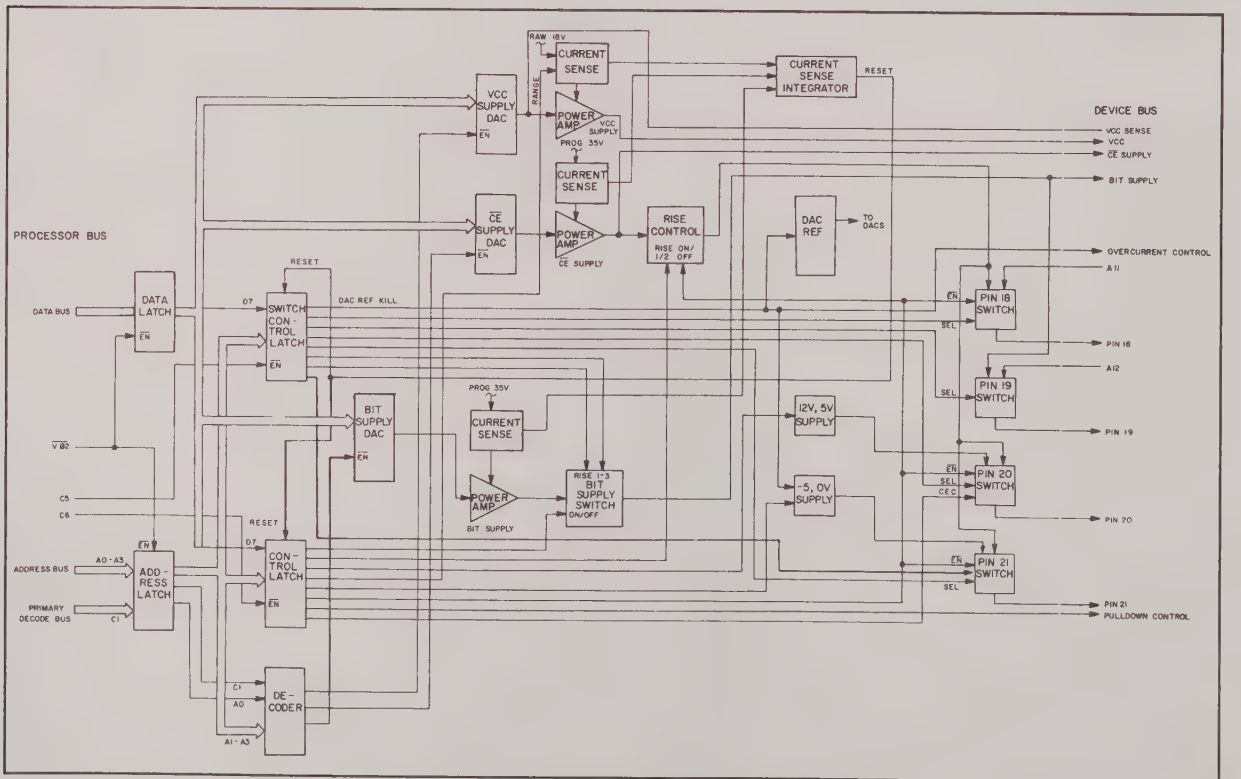


Figure 5-4. Block Diagram, Waveform Generator

The V_{CC} waveforms are generated by writing appropriate DAC values from the firmware. The rise and fall times are fixed by the slewing rate of the op amp. Two overcurrent detectors are included, one for low currents and one for high currents (above 1 amp). If a detector is activated, the control latch is reset; the DAC-reference kill output then causes the DAC reference to go to zero, in turn causing all supplies to return to zero.

The V_{CC} supply senses the V_{CC} voltage at the PROM socket via the V_{CC}-sense line. This remote sensing compensates for all cable drops between the supply and the socket.

The $\overline{CE}$ waveforms are generated by using the $\overline{CE}$ supply in conjunction with one of the pin switches. The voltage level is selected by writing the appropriate value to the $\overline{CE}$ DAC. One of two rise times is selected by the control latch and rise-time control circuitry. Either the pin 18, 20 or 21 switch can be enabled by the switch-control latch to output the high-level $\overline{CS}$ voltage. Switches that are not enabled can output TTL levels.

Each pin switch consists of an emitter follower with the collector tied to the $\overline{CE}$ supply. A current source is provided for the base of each switch to charge the common rise-time capacitor. When the base is released, a linear ramp is generated which is truncated at the $\overline{CE}$-supply level. An NPN-transistor pulldown is included in the switch to provide a 20V/μs-controlled fall time. Logic circuitry prevents the pulldown and pullup circuits from being active simultaneously.

The pin 21 switch uses the same principles as the pin 18 and pin 20 switches. However, a power amplifier output (-5V/0 supply) provides the ground reference for the switch. For certain programming algorithms this amplifier output is brought to -5V.

The pin 20 switch includes a pullup that is connected to the +12/+5V supply, thus allowing the switch in the TTL mode to switch from 0 to 12V as well as from 0 to 5V. The +12/+5V supply consists of a monolithic regulator and a 5.1V zener diode controlled by the switch-control latch.

Signals to be applied to the data lines of a device are generated with the bit-supply signals and controlled by the bit-supply switch. The bit supply is nearly identical to the $\overline{CE}$ supply, but has one less diode in the feedback path, compensating for one less drop in the switch paths. The bit-supply switch consists of an emitter follower, a current source, and three rise-time control capacitors. The collector of the emitter follower is connected to the bit supply; the base is connected to the current source and timing capacitor. The control latch can select the timing capacitor and also control the base of the switch. When the base is released, the output ramps linearly to the bit-supply level. The output on the bit-supply switch is sent to the address and data driver card and to the pin 19 switch. Unlike the pin 18, 20 and 21 switches, the pin 19 switch consists of a simple PNP-saturating switch controlled by the switch-control latch.

The current-sense integrator smoothes the transient overcurrent pulses occurring from charging supply capacitors. When an overcurrent condition from the V_{CC}, $\overline{CE}$, bit or 0/-5V supply exists for sufficient time, the control latch is reset, in turn causing the DAC reference and the supplies to go to zero. The state of the overcurrent-control line can be read by the address and data driver card and used by the programmer to detect shorted devices. Table 5-2 lists the functions of the device-bus pins. The data latch buffers the data bus and holds data to satisfy the long DAC data-hold requirement. The address latch buffers the lower-order address lines and the primary decode bus. These buffered lines are then sent to the decoder and the address latches. The decoder provides decode signals to the DACs for the V_{CC}, $\overline{CE}$ and bit supplies. The switch-control latch and the control latch receive their clocks from a decoder on the address and data driver card.

Table 5-2. Pin Functions, Device Bus (at J1)

1	PA_8	26	PA_7
2	PA_9	27	PA_6
3	PA_{10}	28	PA_5
4	PA_{11}	29	PA_4
5	PA_{12}	30	PA_3
6	PA_{13}	31	PA_2
7	PA_{14}	32	PA_1
8	PA_{15}	33	PA_0
9	GND	34	Vcc
10	Vcc Sense	35	GND
11	CE Supply	36	GND
12	Bit Switch	37	Bit Supply
13	Pin 20	38	Pin 18
14	Pin 21	39	Pin 19
15	Scope Trigger	40	PD_1
16	-9	41	PD_2
17	+24	42	PD_3
18	Overcurrent	43	PD_4
19	Pull Down Control	44	S1
20	Vcc Pullup	45	S2
21	VREF	46	S3
22	PD_8	47	Spare
23	PD_7	48	Spare
24	PD_6	49	+5
25	PD_5	50	GND

5.3.3 Address and Data Driver

The address and data driver, diagrammed in figure 5-5, provides the device address, device data, data loads and supply measurement capability of the UniPak™.

The address drivers consist of addressable latches driving the device address bus. The addressable latches receive data from the most-significant-bit line of the data bus.

The data switch register drives PNP data switches which direct the output of the bit switch to the appropriate device-data line. The PNP switches are driven by current sources to provide a constant-base drive at all bit-switch voltages.

The data sink register drives the NPN data sinks directly. These data sinks are used to shunt to ground large programming currents. Device data is read via the data comparators and strobed to the processor bus via the data gate. The comparators receive their reference voltage from the V_{REF} amplifier, which is controlled by the V_{REF} DAC. Loading the device data bus is controlled by the load DAC, the load amplifier and the high/low-range load switch. A voltage is developed by the load amp and applied to either the high-range or low-range resistor banks. The diode clamps limit the voltage applied by the load resistors to the data bus to approximately 5V.

The supply comparators read the V_{CC}-sense line, the $\overline{CE}$ supply and the bit-switch line. The comparator gate/multiplexer strobes the data from the supply comparators and the overcurrent-read line to the most-significant-bit line of the data bus.

The socket-select latch provides a control line for the high-/low-range switch and control lines for the socket card.

The data latch buffers the data bus and holds data to satisfy the DAC requirements.

The address latch buffers low-order addresses for the secondary decoder. The decoder provides the appropriate signals for the DACs and registers as well as the latches on this card and on the waveform generator. The $\overline{V \bullet \emptyset_2}$ signal controls the timing of the various clock signals developed by the decoder.

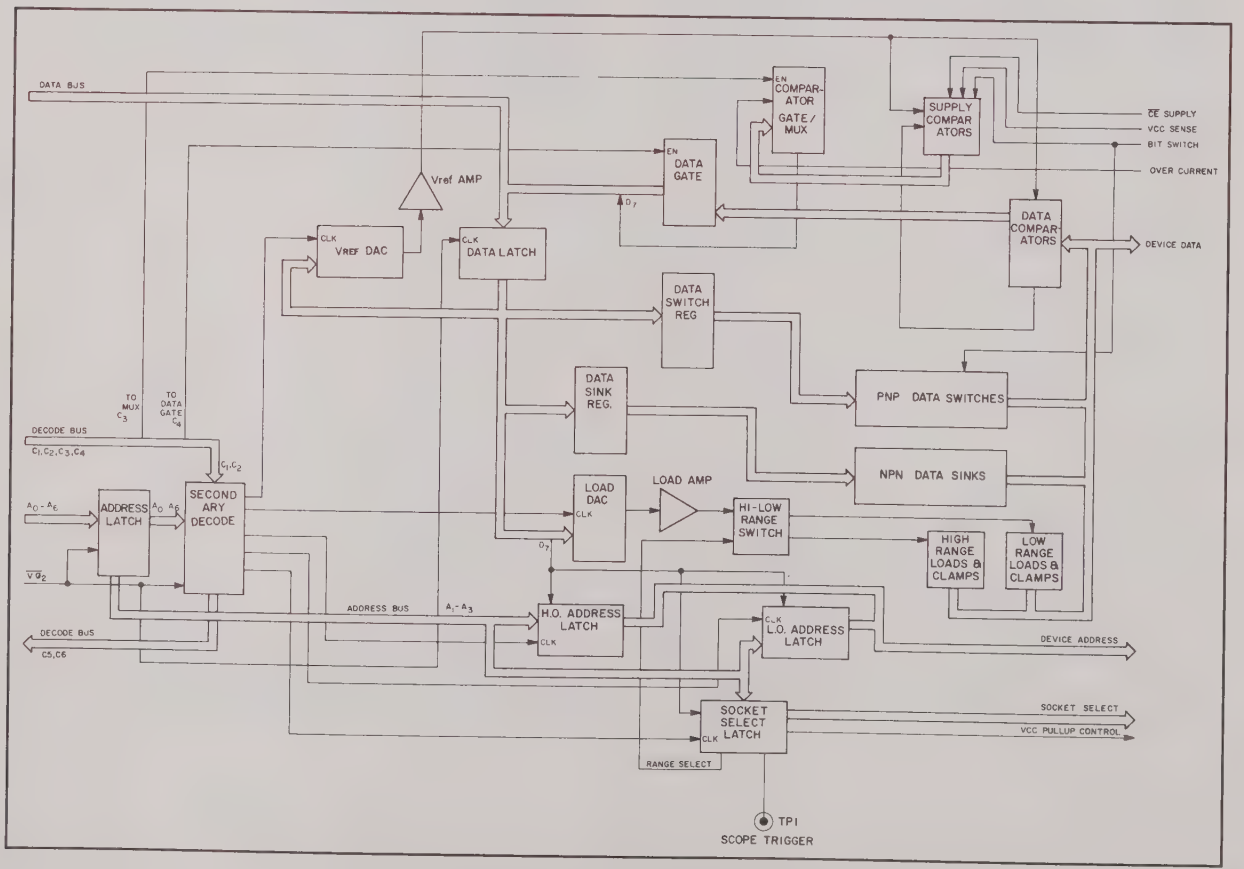


Figure 5-5. Block Diagram, Address and Data Driver Card

5.3.4 UniPak™ Socket Card

The UniPak™ socket card distributes to the device sockets the signals developed on the address and data driver card and the waveform generator. Refer to the block diagram, figure 5-6. The device address lines connect directly to the device sockets; larger devices connect to more device addresses than smaller devices; diode-overvoltage protection on these lines prevents damage to the drivers on the address and data driver card.

The device-data bus connects directly to all sockets. Four-bit devices are connected to PD_1-PD_4. The data pulldowns consist of 1K-ohm resistors and a diode network. Data-spike clamps consist of diode networks and capacitor-resistor networks. The diode networks are used to clip overshoot on the data-line programming pulses. The capacitor network is charged by the bit supply so that the network does not absorb energy from the actual data-line programming pulses.

Pins 18, 19, 20 and 21 of the 24-pin device socket receive signals directly from the waveform generator via the corresponding pin switches. A spike-suppression network similar to that used on the data lines is provided where the $\overline{CE}$ supply charges the RC network. V_{CC} is applied to all sockets through seven diodes. Remote sensing of the voltage at the selected socket is provided by the analog switch of the V_{CC}-sense multiplexer. When V_{CC} is brought to zero, the device's V_{CC} lines can be pulled up by the V_{CC} pullups. The V_{CC} sense-multiplexer and a comparator on the address and data driver card are then used to read the V_{CC} voltage. If a device is properly inserted in a socket, the V_{CC} voltage will be above 2V. If it is in backwards, it will be below 1V, and if no device is in the socket, the voltage will approach 4V.

The LED decoder is used to light the LEDs below the selected socket.

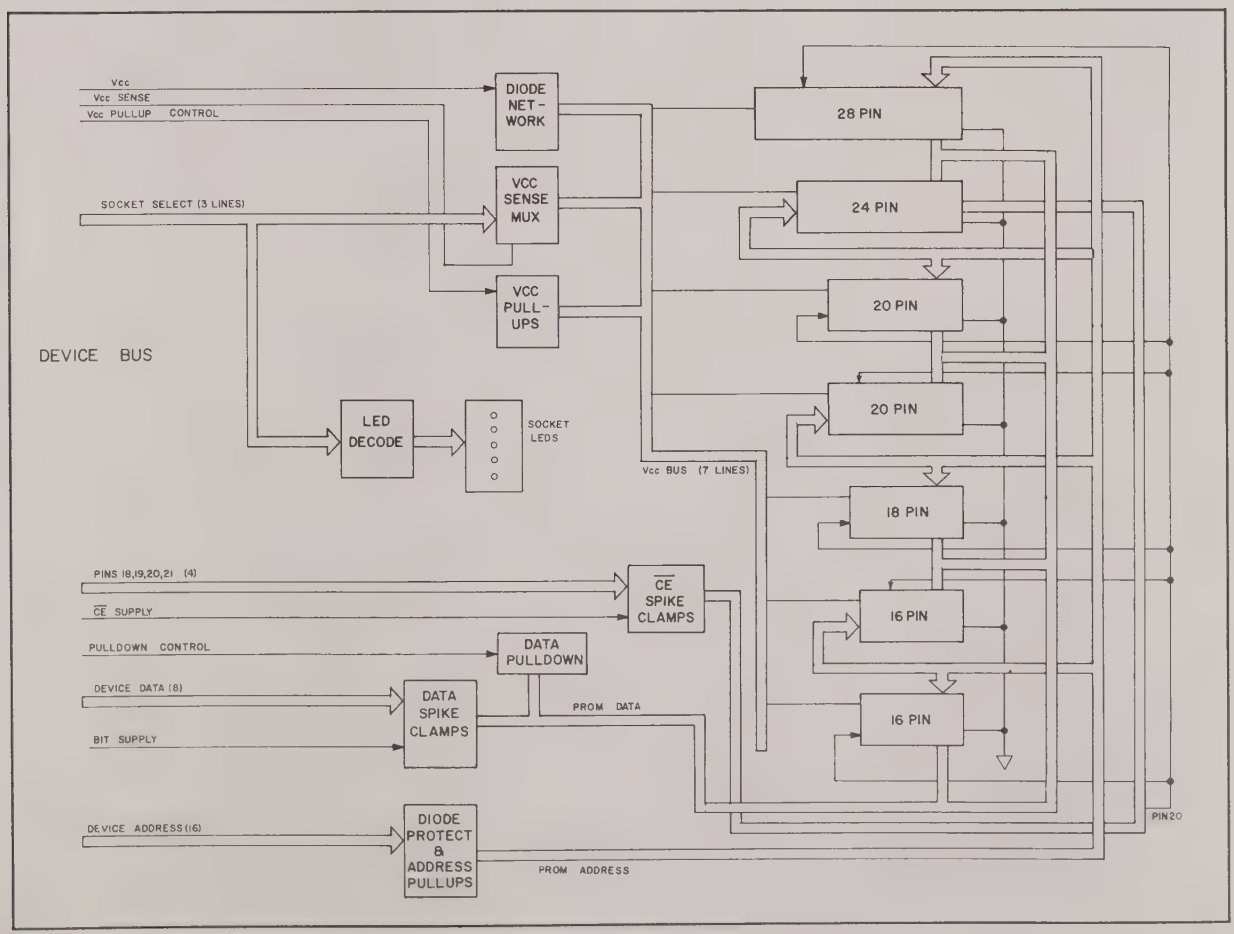


Figure 5-6. Block Diagram, UniPak™ Socket Card

5.3.5 UniPak™ Memory Card

The UniPak™ memory card is shown in block diagram form in figure 5-7. PROMs which store the UniPak™ software are contained on the memory card. These PROMs connect to the address bus directly and to the data bus through data buffers.

Two PROMs and a latch comprise the primary decoder. The PROMs connect to the 12 high-order address lines and the R/$\overline{W}$ line. Outputs from the primary-decoder latch connect to the secondary decoder and also to secondary decoders on the address and data driver card and the waveform generator. A 1-of-8 decoder, timed with $\overline{V \cdot \emptyset_2}$, provides the secondary decoding for the software PROMs. Two additional lines from this decoder connect to the address card to provide the decode signals for the data gate and comparator gate/multiplexer. Additional outputs from the primary decoder enable the data buffer during all software-read operations and lower the data-gate-enable line during any access of the UniPak™

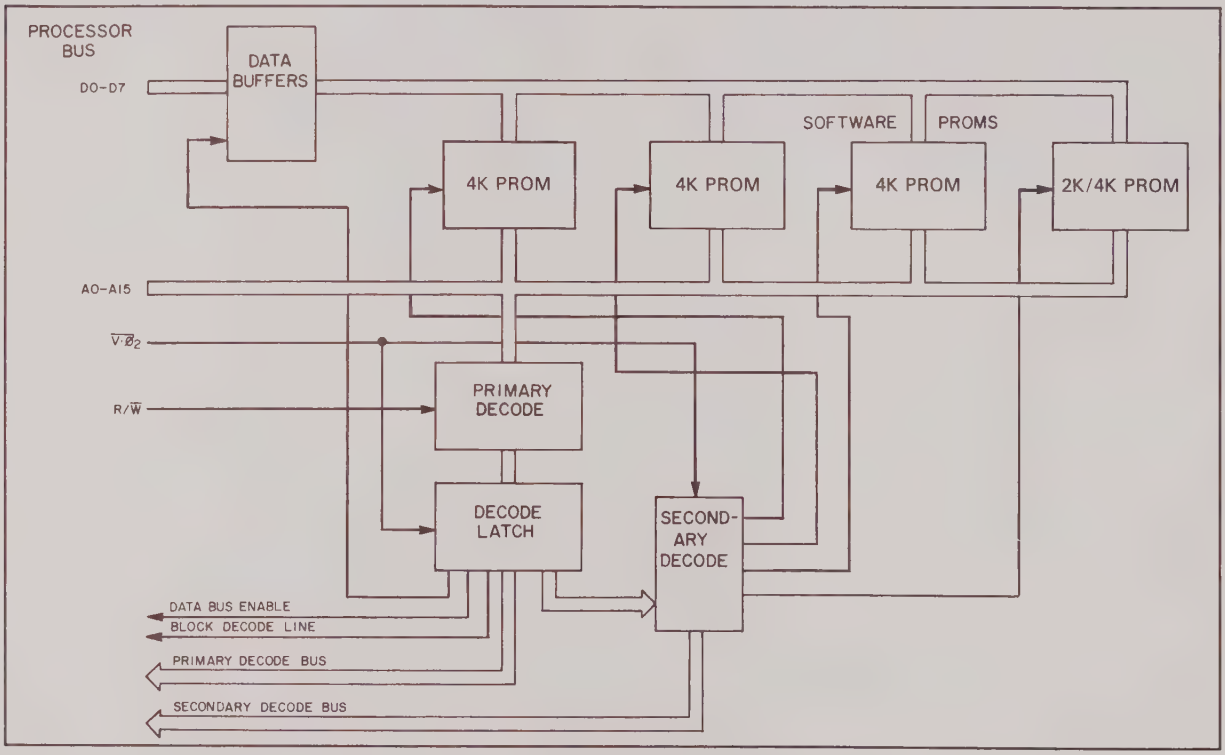


Figure 5-7. Block Diagram, UniPak™ Memory Card

APPENDIX A
FAMILY AND PINOUT CODES
ERROR CODES

KEY TO HEADINGS AND FOOTNOTES

- **Device Part Number.** The number assigned by the device manufacturer.
- **Family Code.** A 2-digit number that designates the programming algorithm.
- **Pinout Code.** A 2-digit number used to differentiate device types based on pin assignment and array size.
- **Software Version.** A number in this column specifies the earliest software version of the 22A that will program the device to the manufacturer's latest specifications.
- **Approval Status.** The following is an explanation of the symbols used in this column.

  A - Written approval obtained.

  O - Device is obsolete and no longer in production. No approval can be obtained. Algorithm has been used and approved in previous Data I/O equipment.

  S - This algorithm is in the process of submission for manufacturer approval. The algorithm has been tested by Data I/O or the manufacturer, but no representation as to yield level is made or implied.

CAUTION

Entry of an invalid family/pinout code, other than those listed in this table can cause unpredictable results at the device socket, which may damage a device. A valid family code and a valid pinout code may be combined to produce an invalid (illegal) combination. The correct combination for your device is published in this table. All family/pinout combinations not contained in this table are considered "illegal". Data I/O assumes no responsibility or liability for results produced by entry of "illegal" family/pinout combinations.

Table A-1. UniPak™ Family and Pinout Codes

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Advanced Micro Devices					
2708	21	27	A	-	A
27128	AF	51	005	-	A
27128A	C1	51	V07	-	A
2716	19	23	A	-	A
27256	C1	32	V07	-	S
2732	19	24	A	-	A
2732A	27	24	005	-	A
27512	DD	A4	V07		A
2764	AF	33	005	-	A
2764A	C1	33	V07		A
27LS18	16	02	A	-	A
27LS185	16	06	E	-	A
27LS19	16	02	A	-	A
27PS181	16	37	A		A
27PS184	16	06	A		A
27PS185	16	06	E		A
27PS191	16	68	H		A
27PS281	16	37	003	-	A
27PS291	16	68	003	-	A
27PS41	16	53	005	351A-065	A
27PS43	16	63	004	-	A
27PS49	16	67	003	-	A
27S08	15	02	A	-	O
27S09	15	02	A	-	O
27S10	15	01	A		O
27S11	15	01	A		O
27S12	16	03	A	-	A
27S13	16	03	A	-	A
27S15	16	79	005	351A-068	A
27S18	16	02	A		A
27S180	16	37	A		A
27S181	16	37	A	-	A
27S184	16	06	E		A
27S185	16	06	E		A
27S19	16	02	A	-	A
27S190	16	68	H	-	A
27S191	16	68	H	-	A
27S20	16	01	A	-	A
27S21	16	01	A	-	A
27S24	16	65	003	-	A
27S25	16	65	003	-	A
27S26	16	85	005	351A-067	A
27S27	16	85	005	351A-067	A
27S28	16	09	E	-	A
27S280	16	37	003		A
27S281	16	37	003	-	A
27S29	16	09	A	-	A
27S290	16	68	003	-	A
27S291	16	68	003	-	A
27S30	16	36	A	-	A
27S31	16	36	A	-	A
27S32	16	38	E	-	A
27S33	16	38	E	-	A
27S35	16	66	004	-	A
27S37	16	66	004		A
27S40	16	53	004	351A-065	A
27S41	16	53	004	351A 065	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Advanced Micro Devices (Continued)					
27S43	16	63	004	-	A
27S45	16	77	004	351A-066	A
27S47	16	77	004	351A-066	A
27S49	16	67	003	-	A
27S65	16	93	V07	351A-073	A
27S75	16	94	V07	351A-073	A
27S85	16	95	V07	351A-073	A
9864	C9	A6	V07	-	A
9864 3	C9	A6	V07	-	S
29750A	16	02	A		A
29751A	16	02	A	-	A
29760A	16	01	A	-	A
29761A	16	01	A		A
29770	16	03	A	-	A
29771	16	03	A	-	A
29774	16	85	005	351A-067	S
29775	16	85	005	351A-067	S
AM9708	21	27	A		A
AM9716	19	23	A	-	A
AM9732	19	24	A	-	A
AM9764	AF	33	005	-	A
Electronic Arrays					
2708	21	27	A	-	A
2716	19	23	A	-	A
Eurotechnique					
ET2716	19	23	005	-	A
ET2732	19	24	005	-	A
ETC2716	19	23	005	-	A
ET2764	35	33	V07	-	S
Exel					
2816A	B7	23	V07	-	S
Fairchild					
2708	21	27	A	-	A
93417	01	01	A	-	A
93427	01	01	A	-	A
93436	01	03	A	-	A
93438	01	15	A	-	A
93446	01	03	A		A
93448	01	15	A	-	A
93450	01	16	A		A
93451	01	16	A		A
93452	01	05	A	-	A
93453	01	05	A	-	A
93460	01	16	A	-	A
93461	01	16	A	-	A
93510	01	21	004	-	A
93511	01	21	004	-	A
93514	01	06	A	-	A
93515	01	06	A	-	A
93L450	01	16	A	-	A
93L451	01	16	A	-	A
Fujitsu					
27128	45	51	005	-	S
2732A	27	24	F	-	A
2732A-35	27	24	C	-	A
2764	45	33	005	-	A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Fujitsu (Continued)					
27C128	45	51	005	-	S
27C256	45	32	V07	-	S
27C32A	27	24	A	-	A
27C64	45	33	005	-	A
8516	19	23	E	-	A
8518	21	27	E	-	A
8532	19	24	F	-	A
8742	50	57	005	351A-070	S
8749H	50	57	005	351A-070	S
General Instruments					
5716	83	23	003	-	A
5816	37	23	003	-	A
Harris					
6641	40	47	F	-	A
7602	05	02	A	-	A
7603	05	02	A	-	A
7608	05	16	A	-	A
7610	05	01	A	-	A
7611	05	01	A	-	A
7616	05	42	A	-	A
76160	05	21	A		O
76161	05	21	A	-	A
76165	05	53	004	351A-065	A
7620	05	03	A	-	A
7621	05	03	A	-	A
7629	05	43	A	-	O
76320	05	63	H	-	O
76321	05	63	H		A
7640	05	15	A		A
7641	05	15	A	-	A
7642	05	05	A	-	A
7642P	05	38	H		O
7643	05	05	A	-	A
7643P	05	38	H	-	O
7644	05	04	A	-	O
7647R	05	79	V07	351A-068	S
7648	05	09	A	-	A
7649	05	09	A	-	A
76641	05	67	H	-	A
7680	05	16	A		A
7680RP	05	16	H	-	O
7681	05	16	A	-	A
7681RP	05	16	H	-	O
7684	05	06	A	-	A
7684P	05	06	H	-	O
7685	05	06	A	-	A
7685P	05	06	H	-	O
7686	05	10	A		A
7687	05	10	V01	-	A
Hitachi					
27C32	19	24	A	-	O
27C32A	27	24	A	-	O
462532	19	25	E	-	A
462716	19	23	F	-	A
462732	19	24	F		A
462732P	19	24	A		A
48016	33	23	E		A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Hitachi (Continued)					
4827128	79	51	004	-	A
482732A	27	24	A	-	A
482764	79	33	004	-	A
Hughes					
3004-1	58	62	004	-	A
3004-2	58	61	004	-	A
3008	58	60	004	-	A
3104-1	58	62	004	-	A
3104-2	58	61	004	-	A
3108	58	60	004	-	A
Intel					
2704	21	26	A	-	O
2708	21	27	A	-	O
27128	79	51	004	-	A
27128A	93	51	005	-	A
2716	19	23	A	-	A
27256	93	32	005	-	A
2732	19	24	A	-	A
2732A	27	24	A	-	A
27512	4B	A4	V09	-	S
2758	19	22	A	-	A
2764	79	33	004		A
2764A	93	33	005		A
2815	85	23	005	-	A
27C64	93	33	V05	-	S
2816	37	23	H	-	A
2816A	A5	96	V07	-	A
2817A	BF	A2	V07	-	A
8704	21	26	A	-	A
8708	21	27	A	-	A
8741	56	59	005	351A-070	S
8741A	56	59	005	351A-070	S
8742	50	57	V07	351A-070	S
8744	53	58	V04	351A-071	S
8748	52	56	005	351A-070	S
8748H	50	56	005	351A-070	S
8749H	50	57	005	351A-070	S
8751	53	58	005	351A-071	S
8751H	D5	58	V07	351A-071	S
8755A	47	55	005	351A-072	S
Intersil					
6716	59	64	004	-	A
Mitsubishi					
2708	21	27	A	-	A
27128	79	51	004	-	S
2716	19	23	A		A
2732	19	24	A	-	A
2732A	27	24	A	-	A
2764	79	33	004	-	A
8748	52	56	V07	351A-070	S
Monolithic Memories					
5300	11	01	D	-	A
	E5	01	V09	-	S

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
5301	11	01	D	-	A
	E5	01	V09	-	S
5305	11	03	D	-	A
	E5	03	V09	-	S
5306	11	03	D	-	A
	E5	03	V09	-	S
5308	11	08	D	-	A
	D1	08	V07	-	A
5309	11	08	D	-	A
	D1	08	V07	-	A
5330	29	02	D	-	A
	E7	02	V09	-	S
5331	29	02	D	-	A
	E7	02	V09	-	S
5335	11	14	D	-	A
	D1	14	V07	-	A
5336	11	14	D		A
	D1	14	V07	-	A
5340	11	15	D	-	A
	D1	15	V07	-	A
5340JS	11	15	D	-	A
	D1	15	V07	-	A
5341	11	15	D	-	A
	D1	15	V07	-	A
5341JS	11	15	D	-	A
	D1	15	V07		A
5348	11	09	D	-	A
	D1	09	V07	-	A
5349	11	09	D		A
	D1	09	V07		A
5352	11	05	D	-	A
	D1	05	V07	-	A
5353	11	05	D	-	A
	D1	05	V07	-	A
5380	11	16	D	-	A
	D1	16	V07	-	A
5380JS	11	16	D	-	A
	D1	16	V07	-	A
5381	11	16	D	-	A
	D1	16	V07		A
5381JS	11	16	D	-	A
	D1	16	V07	-	A
5388	11	06	D	-	A
	D1	06	V07	-	A
5389	11	06	D	-	A
	D1	06	V07	-	A
53LS080	18	02	004	-	O
53LS081	18	02	004	-	O
53S080	18	02	004	-	O
53S081	18	02	004	-	O
6300	11	01	D	-	A
	E5	01	V09	-	S
6301	11	01	D	-	A
	E5	01	V09	-	S
6305	11	03	D		A
	E5	03	V09	-	S

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
6306	11	03	D	-	A
	E5	03	V09	-	S
6308	11	08	D	-	A
	D1	08	V07	-	A
6309	11	08	D	-	A
	D1	08	V07	-	A
6330	29	02	D	-	A
	E7	02	V09	-	S
6331	29	02	D	-	A
	E7	02	V09	-	S
6335	11	14	D	-	A
	D1	14	V07	-	A
6336	11	14	D	-	A
	D1	14	V07	-	A
6340	11	15	D	-	A
	D1	15	V07	-	A
6340JS	11	15	D	-	A
	D1	15	V07	-	A
6341	11	15	D	-	A
	D1	15	V07	-	A
6341JS	11	15	D	-	A
	D1	15	V07	-	A
6348	11	09	D	-	A
	D1	09	V07	-	A
6349	11	09	D	-	A
	D1	09	V07	-	A
6352	11	05	D	-	A
	D1	05	V07	-	A
6353	11	05	D	-	A
	D1	05	V07	-	A
6380	11	16	D	-	A
	D1	16	V07	-	A
6380JS	11	16	D	-	A
	D1	16	V07	-	A
6381	11	16	D	-	A
	D1	16	V07	-	A
6381JS	11	16	D	-	A
	D1	16	V07	-	A
6388	11	06	D	-	A
	D1	06	V07	-	A
6389	11	06	D	-	A
	D1	06	V07	-	A
63D1641	B2	80	V07	351A-073	A
63D1642	B2	80	V07	351A-073	A
63DA1643	AA	87	V07	351A-073	A
63DA441	AA	AC	V07	351A-073	A
63DA841	AA	AD	V07	351A-073	A
63DS1643	AA	87	V07	351A-073	A
63LS080	18	02	004	-	A
63LS081	18	02	004	-	A
63LS140	18	01	004	-	A
63LS141	18	01	004	-	A
63LS240	18	03	004	-	A
63LS241	18	03	004	-	A
63PL1681	18	21	V07	-	A
63PS1681	18	21	005	-	A
63RA1681	18	A3	V07	-	A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Monolithic Memories (Continued)					
63RA441	18	07	004	-	A
63RA481	EC	65	V09		S
63RA841	18	11	004	-	A
63RS1681	18	A3	V07	-	A
63RS881	18	86	005	-	A
63S080	18	02	004	-	A
63S081	18	02	004	-	A
63S140	18	01	004	-	A
63S141	18	01	004	-	A
63S1640	18	53	004	351A 065	A
63S1641	18	53	005	351A-065	A
63S1680	18	21	004	-	A
63S1681	18	21	004	-	A
63S1681J	18	21	004	-	A
63S240	18	03	004		A
63S241	18	03	004	-	A
63S3281	18	63	005	-	A
63S440	18	05	004	-	A
63S441	18	05	004	-	A
63S480	18	09	004		A
63S481	18	09	004	-	A
63S840	18	06	004	-	A
63S841	18	06	004	-	A
63S881	18	16	004		A
Mostek					
2716	19	23	A	-	A
Motorola					
68732-0	25	44	A	-	O
68732-1	25	45	A	-	O
76161	05	21	A		A
76165	05	53	003	351A-065	S
7620	05	03	A	-	O
7621	05	03	A		A
7640	05	15	A	-	O
7641	05	15	A	-	A
7642	05	05	A	-	O
7643	05	05	A	-	A
7649	05	09	A	-	A
7680	05	16	A	-	O
7681	05	16	A	-	A
7684	05	06	A	-	O
7685	05	06	A	-	A
MCM2532	19	25	B	-	A
6836E16	2D	5A	V09	-	S
MCM2708P	21	27	A	-	O
MCM2716	19	23	B	-	A
MCM2808	81	72	003	-	A
MCM2816	43	23	003		A
MCM2817	81	71	003	-	A
MCM2832	81	70	003	-	A
MCM68708	21	27	A	-	A
MCM68764	25	29	F	-	A
MCM68766	25	29	F	-	A
TMS2716	23	28	A	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
National Semiconductor					
2532	19	25	A	-	A
25C32	19	25	A	-	A
2708	21	27	A		A
2716	19	23	A	-	A
2732	19	24	A	-	A
2758A	19	22	A	-	A
2758B	19	35	A	-	A
2764	35	33	F	-	S
2764H	63	33	V07		S
27C16	19	23	E	-	A
27C16H	BD	23	V07	-	S
27C32	19	24	A		A
2864	C7	A5	V09		S
27C32H	BD	24	V07	-	S
2816	37	23	003	-	A
54LS471	08	08	A	-	O
54S188	08	02	A		O
54S287	08	01	A		O
54S288	08	02	A	-	O
54S387	08	01	A	-	O
54S471	08	08	A	-	O
54S472	08	09	A	-	O
54S473	08	09	A	-	O
54S474	08	15	A	-	A
54S475	08	15	A	-	A
54S570	08	03	A	-	O
54S571	08	03	A	-	O
54S572	08	05	A	-	A
54S573	08	05	A	-	A
74LS471	08	08	A	-	A
74S188	08	02	A	-	A
74S287	08	01	A	-	A
74S288	08	02	A	-	A
74S387	08	01	A		A
74S471	08	08	A	-	A
74S472	08	09	A	-	A
74S473	08	09	A	-	A
74S474	08	15	A	-	A
74S475	08	15	A	-	A
74S570	08	03	A	-	A
74S571	08	03	A	-	A
74S572	08	05	A	-	A
74S573	08	05	A	-	A
74S574	08	34	A	-	A
77LS181	08	16	A	-	A
77S180	08	16	A		A
77S184	08	06	A	-	A
77S185	08	06	A	-	A
87LS181	08	16	A	-	A
87S180	08	16	A	-	A
87S181	08	16	A	-	A
87S184	08	06	A		A
87S185	08	06	A	-	A
87S190	08	21	A	-	A
87S191	08	21	A	-	A
87S195	08	53	004	-	A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family	Pinout	Software Version	Adapter	Approval Status
National Semiconductor (Continued)					
87S280	08	16	003	-	A
87S281	08	16	003	-	A
87S290	08	21	003	-	A
87S291	08	21	003	-	A
87S295	08	15	A	-	A
87S296	08	15	A	-	A
87S321	08	63	004	-	A
87SR181	08	66	V07	-	A
87SR25	08	81	005	-	A
87SR191	08	77	V09	351A-066	S
87SR474	08	81	V07	-	A
9716	B3	23	005	-	A
87SR27	08	85	V09	351A-067	S
Nippon Electric Company, Ltd.					
27128	79	51	004	-	S
2716	19	23	F	-	A
2732	19	24	F	-	A
2732A	27	24	A	-	A
2764	79	33	004	-	S
8741AD	56	59	005	351A-070	S
8748AD	52	56	005	351A-070	S
8755A	47	55	005	351A-072	S
Oki					
2532	19	25	A	-	A
2708	21	27	A	-	A
27128	79	51	004	-	S
2716	19	23	A	-	A
2732	19	24	A	-	A
2732A	27	24	A	-	A
2758	19	22	A	-	A
2764	79	33	004	-	S
8755A	47	55	005	351A-072	S
Raytheon					
29600	11	08	D	-	A
29601	11	08	D	-	A
29602	11	08	D	-	A
29603	11	08	D	-	A
29610	11	03	D	-	A
29611	11	03	D	-	A
29612	11	03	D	-	A
29613	11	03	D	-	A
29620	11	09	D	-	A
29621	11	09	D	-	A
29622	11	09	D	-	A
29623	11	09	D	-	A
29624	11	15	D	-	A
29625	11	15	D	-	A
29626	11	15	D	-	A
29627	11	15	D	-	A
29630	11	16	D	-	A
29630SM	11	16	003	-	A
29631	11	16	D	-	A
29631SM	11	16	003	-	A
29632	11	16	D	-	A
29632SM	11	16	003	-	A
29633	11	16	D	-	A
29633SM	11	16	003	-	A

Device Part Number	Family	Pinout	Software Version	Adapter	Approval Status
Raytheon (Continued)					
29634	11	16	D	-	A
29635	11	16	D	-	A
29636	11	16	D	-	A
29637	11	16	D	-	A
29640	11	53	004	351A-065	A
29641	11	53	004	351A-065	A
29642	11	53	004	351A-065	A
29643	11	53	004	351A-065	A
29650	11	06	D	-	A
29651	11	06	D	-	A
29652	11	06	D	-	A
29653	11	06	D	-	A
29660	11	01	D	-	A
29661	11	01	D	-	A
29662	11	01	D	-	A
29663	11	01	D	-	A
29671	11	63	H	-	A
29673	11	63	H	-	A
29680	11	21	D	-	A
29680SM	11	21	003	-	A
29681	11	21	D	-	A
29681SM	11	21	003	-	A
29682	11	21	D	-	A
29682SM	11	21	003	-	A
29683	11	21	D	-	A
29683SM	11	21	003	-	A
Ricoh					
RD5H32	27	24	F	-	A
Rockwell					
R87C32	27	24	V07	-	S
87C64	93	33	V07	-	S
Seeq					
27C256	93	32	V07	-	S
5133	79	33	005	-	A
5133H	79	33	005	-	A
5143	79	51	005	-	S
2816A	B7	23	V07	-	S
2816AH	DF	23	V09	-	S
5516A	B7	23	V07	-	S
5516AH	DF	23	V09	-	S
2817A	BF	A2	V07	-	S
5517A	BF	A2	V07	-	S
2817AH	BF	A2	V07	-	S
5517AH	BF	A2	V07	-	S
5213	A5	96	V07	-	A
5213H	B9	96	V07	-	A
52B13	A5	96	V07	-	A
52B13H	B9	96	V07	-	A
52B23	AB	97	V07	-	A
52B23H	F1	97	V07	-	A
52B33	AB	98	V07	-	A
52B33H	F1	98	V07	-	A
SGS Technology					
2532	19	25	003	-	A
2716	19	23	V03	-	A
2764	35	33	V07	-	A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Signetics					
2708	21	27	A	-	A
82123	10	02	A	-	A
82LS135	10	08	A	-	A
82LS137	10	05	A	-	A
82HS195	CF	53	V09	351A-065	S
82LS180	10	16	A	-	A
82LS181	10	16	003	-	A
82PS180	10	16	A	-	A
82PS181	10	16	003	-	A
82HS321	CF	63	V09	-	S
82S123	10	02	A	-	A
82S126	10	01	A	-	A
82S129	10	01	A	-	A
82S130	10	03	A	-	A
82S131	10	03	A	-	A
82S135	10	08	A	-	A
82S136	10	05	A	-	A
82S137	10	05	A	-	A
82S140	10	15	A	-	A
82S141	10	15	A	-	A
82S146	10	09	A	-	A
82S147	10	09	A	-	A
82S180	10	16	A	-	A
82S181	10	16	A	-	A
82S182	10	16	A	-	A
82S183	10	16	A	-	A
82S184	10	06	A	-	A
82S185	10	06	A	-	A
82S190	10	21	A	-	A
82S191	10	21	A	-	A
82S195	10	53	004	351A-065	A
82S23	10	02	A	-	A
82S2708	10	16	A	-	A
82S321	10	63	004	-	A
27C64	35	33	F	-	S
Synertek					
2716	19	23	A	-	A
Texas Instruments					
14S10	03	01	A	-	A
14SA10	03	01	A	-	A
18S030	04	02	A	-	A
18S22	04	08	A		A
18S42	04	09	A	-	A
18S46	04	15	A	-	A
18SA030	04	02	A	-	A
18SA22	04	08	A	-	A
18SA42	04	09	A	-	A
18SA46	04	15	A		A
24S10	13	01	A		A
24S166	13	53	005	351A-065	S
24S41	13	38	A	-	A
24S81	13	06	A	-	A
24SA10	13	01	A	-	A
24SA166	13	53	005	351A-065	S
24SA41	13	38	A	-	A
24SA81	13	06	A	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Texas Instruments (Continued)					
2508	19	22	A	-	A
2516	BD	23	V07	-	A
2532	BD	25	V07	-	A
2564	BD	30	V07	-	A
25L32	19	25	A	-	A
2708	21	27	A	-	A
27128	79	51	005	-	S
2732	BD	24	V07	-	A
2732A	63	24	V07	-	A
2764	79	33	F	-	S
27L08	21	27	A	-	A
28L166	13	21	G	-	A
28L22	13	46	G	-	A
28L42	13	09	G	-	A
28L45	13	15	G	-	S
28L85	13	16	G	-	S
28L86	13	16	A	-	A
28LA22	13	46	G	-	A
28P166	13	21	G	-	S
28P42	13	09	G	-	S
28P45	13	15	G	-	S
28P85	13	16	G	-	S
28S166	13	21	G	-	A
28S2708	13	16	A	-	A
28S42	13	09	A	-	A
28S45	13	15	G	-	A
28S46	13	15	G	-	A
28S85	13	16	G	-	S
28S86	13	16	A	-	A
28SA166	13	21	G	-	S
28SA42	13	09	G		A
28SA46	13	15	G	-	A
28SA86	13	16	A	-	A
54LS478	13	16	A	-	O
54S476	13	38	A	-	A
54S477	13	38	A	-	A
54S478	13	16	A	-	A
54S479	13	16	A	-	A
74188A	04	02	A	-	O
74S188	04	02	A	-	A
74S2708	13	16	A	-	O
74S287	03	01	A	-	O
74S288	04	02	A	-	O
74S387	03	01	A	-	O
74S454	13	06	A	-	O
74S455	13	06	A	-	O
74S470	04	08	A	-	O
74S471	04	08	A	-	O
74S472	04	09	A	-	O
74S473	04	09	A		O
74S474	04	15	A	-	O
74S475	04	15	A	-	O
74S476	13	38	A	-	O
74S477	13	38	A	-	O
74S478	13	16	A	-	O
74S479	13	16	A	-	O
TMS2716	23	28	A		A

Table A-1. UniPak™ Family and Pinout Codes (Continued)

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Thompson					
71190	92	21	004	-	A
71191	92	21	004	-	A
Toshiba					
27128	79	51	004	-	S
2732	19	24	A	-	A
2732A	27	24	A	-	A
2732D	19	24	A	-	A

Device Part Number	Family and Pinout Codes		Software Version	Adapter	Approval Status
Toshiba (Continued)					
2764	79	33	004	-	S
321	21	26	A	-	A
322	21	27	A	-	A
323	19	23	A	-	A
8755AC	47	55	005	351A-072	S
Xicor					
2804A	B7	82	V07	-	S
2816A	B7	23	V07	-	S
2864A	C3	98	V07	-	S

Table A-2. Error Codes*

CODE	NAME	DESCRIPTION
21	Illegal-Bit Error	The device cannot be programmed due to already programmed locations of incorrect polarity.
23	First-Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during device programming.
24	Second-Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during device programming.
27	Insufficient RAM	Due to the value of the Begin RAM Address, there is insufficient RAM to program the device, or the total allotment of RAM resident is less than the word limit of the device.
30	No Programming Algorithm	Valid family and pinout codes are not selected, or family code selection is not followed by pinout code selection.
31	Excessive Current Drain	The operation aborted due to excessive current drain by a device.
32	Backward Device	The operation aborted due to V_{CC} level test indicating a backward device.
35	Faulty Chip Select	The operation aborted due to data being present while a device is disabled.
37	Socketing Error	Operation aborted due to a low V_{CC} level indication on sockets presumed to be empty. A device may be in the wrong socket, or two or more devices may be socketed simultaneously.
38	Illegal Operation During Calibration	An illegal or invalid operation was attempted during calibration.
39	Failure to Lock Security Fuse	The security bit did not program and the device is not locked.
70	Faulty Bit Supply	The operation aborted due to a faulty bit supply. Do not use UniPak™ until repaired.
71	Faulty CS Supply	The operation aborted due to a faulty CS supply. Do not use UniPak™ until repaired.
72	Faulty V_{CC} Supply	The operation aborted due to a faulty V_{CC}. Do not use UniPak™ until repaired.
B0	Byte Erase Error	The device does not have a byte erase mode. Block limits must be removed and a chip erase performed. The entire chip may then be reprogrammed.
B1	Chip Erase Error	The device does not have a chip erase mode.

*In the case of an error condition, be sure that the family and pinout codes are correct for the PROM installed; refer to table A-1 in this appendix to cross check family and pinout codes.

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FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.5	5.8	6.1	V	Not Shown
	VPP	20.0	20.5	21.0	V	
	VPPN	5.7	5.9	6.1	V	
	TPW	45	50	55	ms	
	T_R	50			µs	
	T_F	50			µs	
	Reject		4		Pulses	See note 3
	Overprogram		1		Pulses	See note 3
1ST PASS VERIFY	V_{CC}	4.8	4.9	5.0	V	
	V_{REF}	0.7	0.8	0.9	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	16.5	17.5	18.5	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	3.4	3.5	3.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	19.2	20.2	21.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 59.*
2. *Load RAM with hex 01 for Family 60, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Pulse 2 of the 4-pulse string is actually an overprogram pulse.*

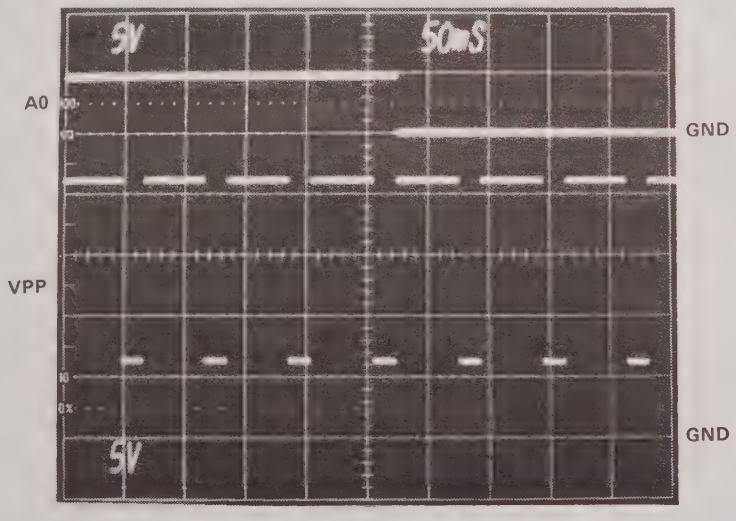
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

TIMING DIAGRAM

FAMILY CODES 59, 60

DATA I/O



5

B-127
981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

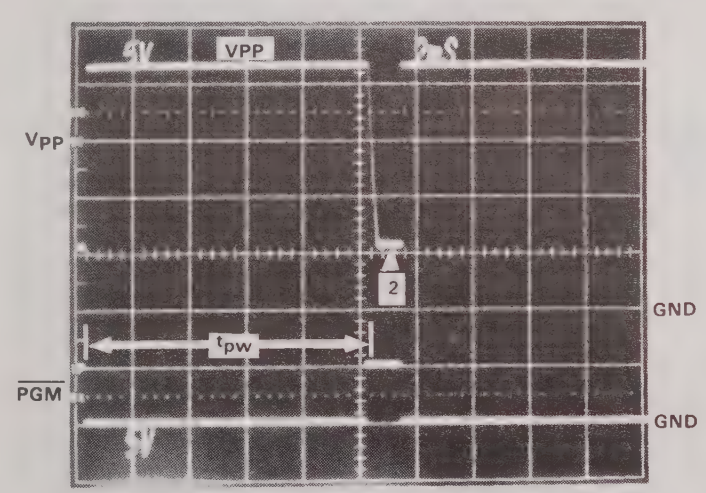
Sheet 2 of 2

TIMING DIAGRAM

FAMILY CODES 59, 60

DATA I/O

0526/1282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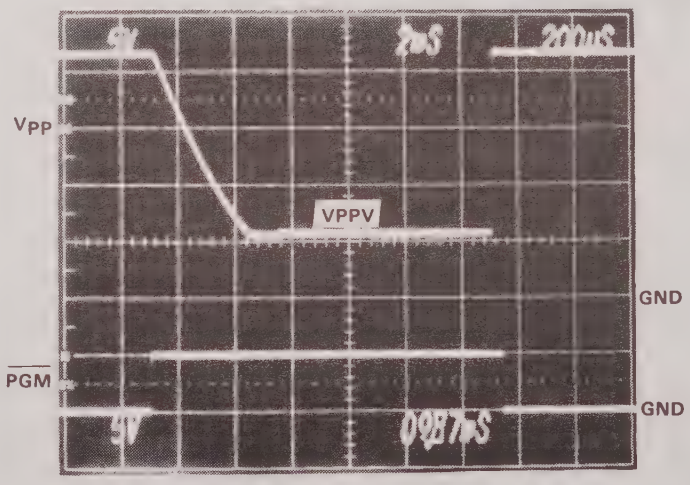
VPP
2mS
VPP
2
GND
tpw
PGM
GND
5V

1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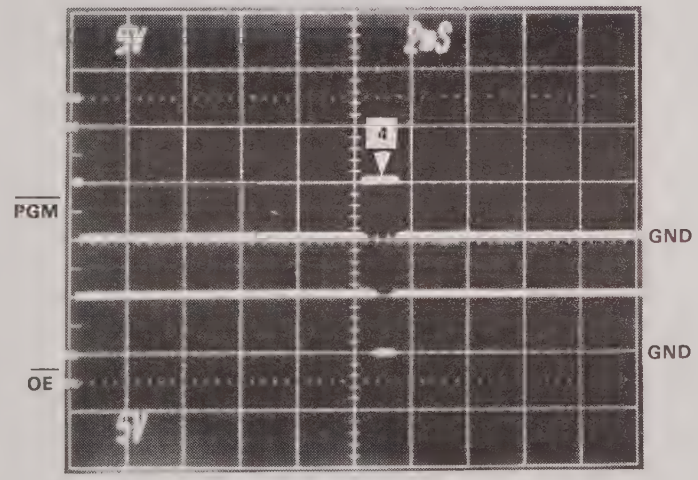
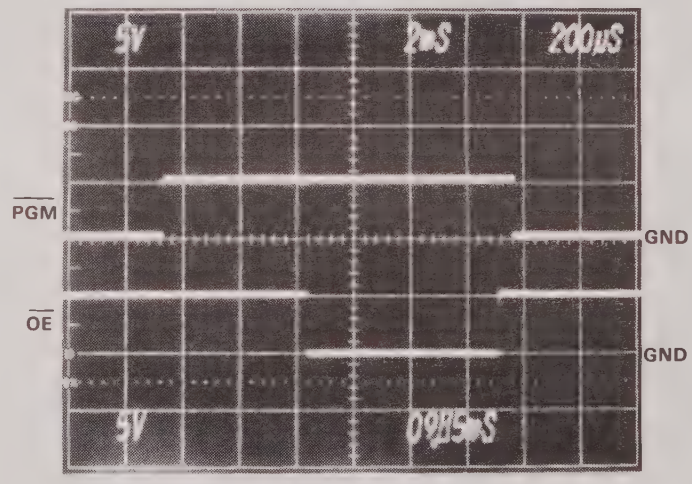
2mS
200µS
VPP
VPPV
GND
PGM
GND
5V

2


5V
2mS
4
PGM
GND
GND
OE
5V

3


5V
2mS
200µS
PGM
GND
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PPV}	4.75	5.0	5.25	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 63.*
2. *Photos 7 and 8 are for Pinout 24.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

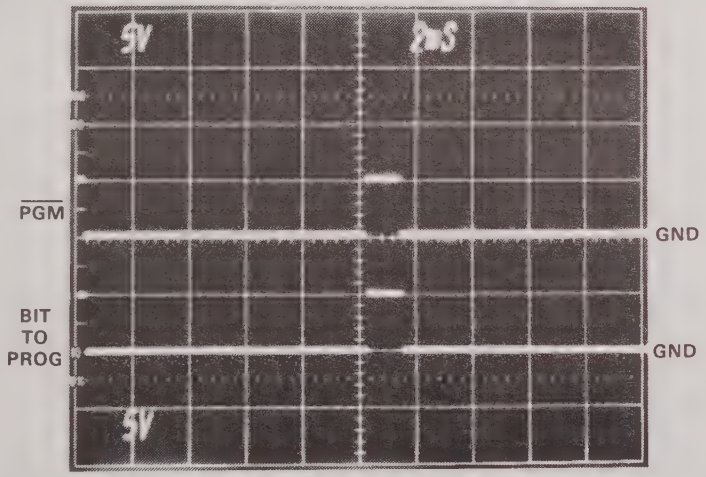
Sheet 1 of 2

TIMING DIAGRAM

FAMILY CODES 63, 64

DATA I/O

0526/1282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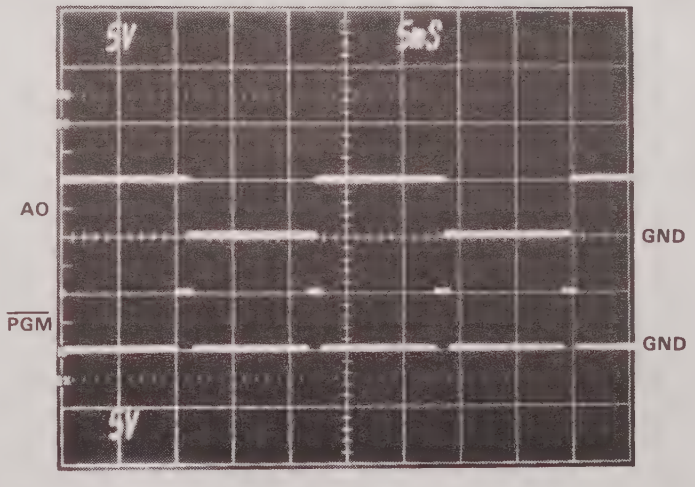
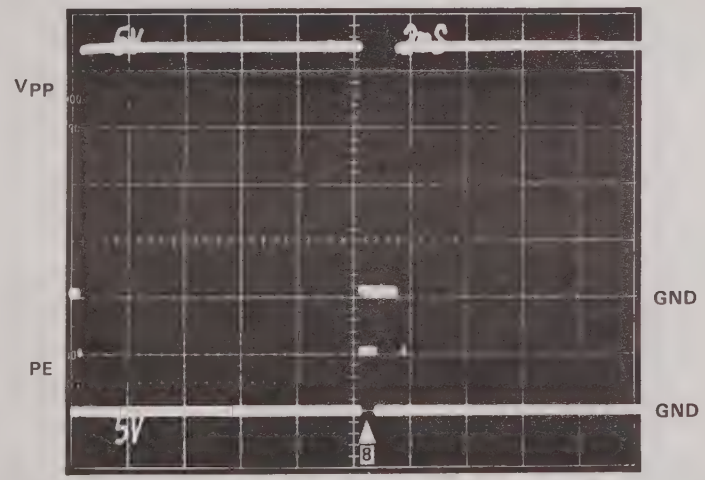
2mS
PGM
GND
BIT
TO
PROG
GND
5V

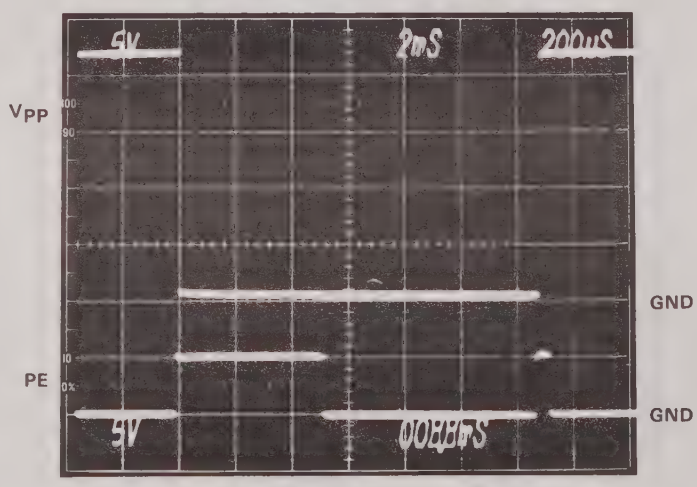
5


5V
5mS
AO
GND
PGM
GND
5V

6


5V
2mS
VPP
GND
PE
GND
5V

7


5V
2mS
200uS
VPP
GND
PE
GND
5V
GND

8

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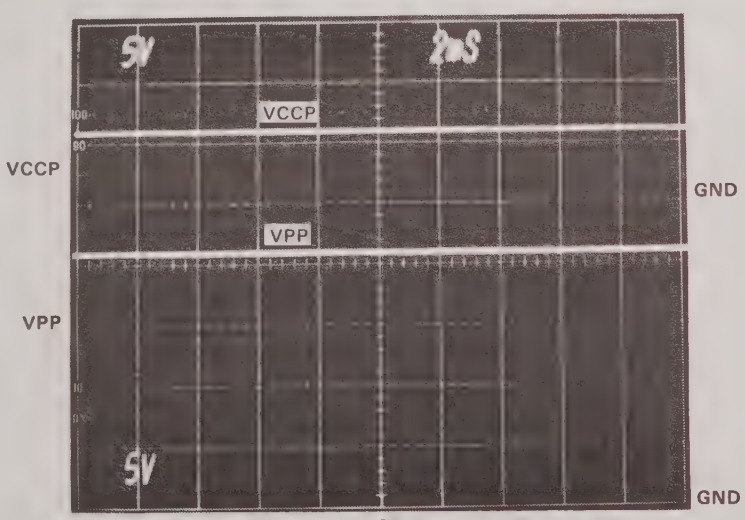
TIMING DIAGRAM

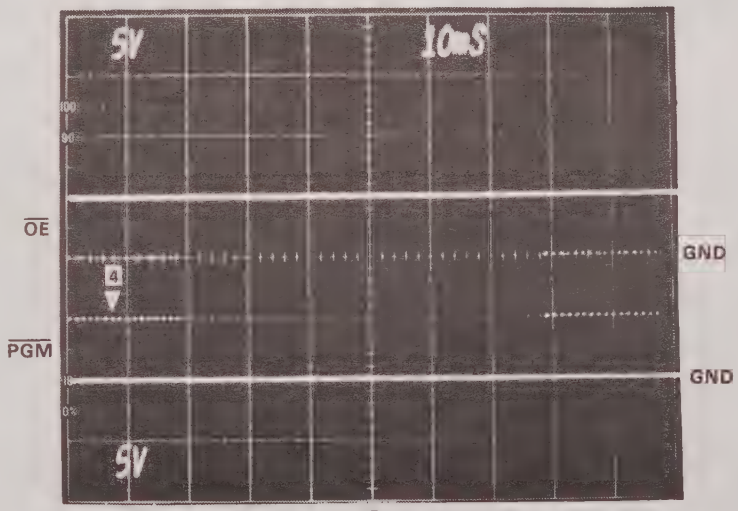
FAMILY CODES 63, 64

DATA I/O

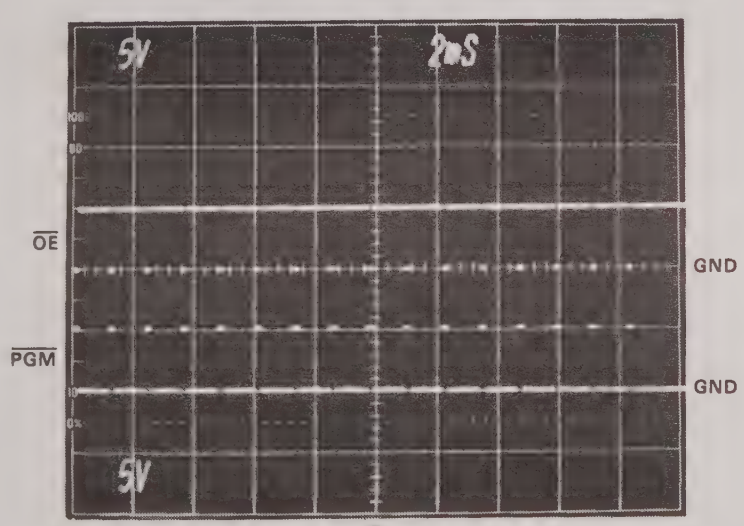
0526/1282


5V
2mS
VCCP
VPP
VCCP
VPP
GND
GND
5V

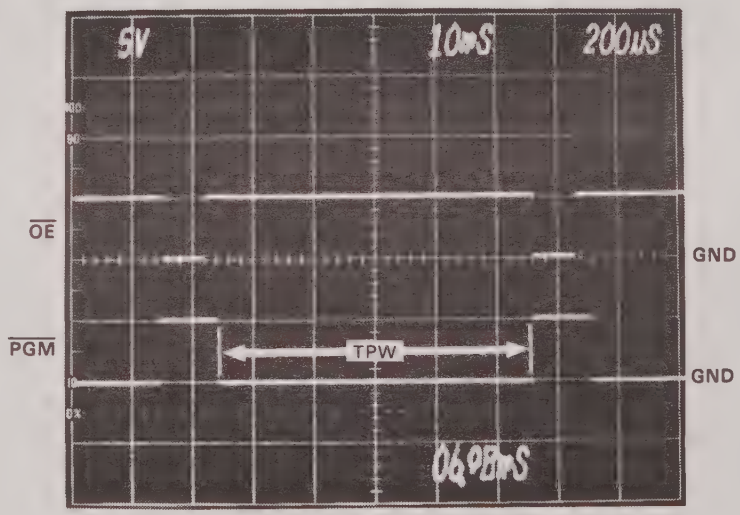
1


5V
10mS
OE
PGM
GND
GND
5V

2


5V
2mS
OE
PGM
GND
GND
5V

3


5V
10mS
200uS
OE
PGM
TPW
GND
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.0	6.25	V	
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		15		Pulses	
	Overprogram		1		Pulses	See Note 3
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 79.*
2. *Load RAM with hex 01 for Family 80, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse follows the reject pulses and its length is the number of reject pulses multiplied by 4 ms.*

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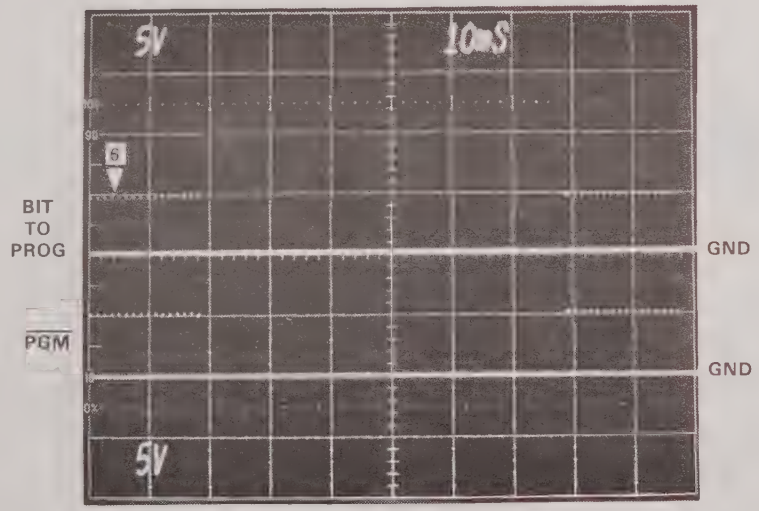
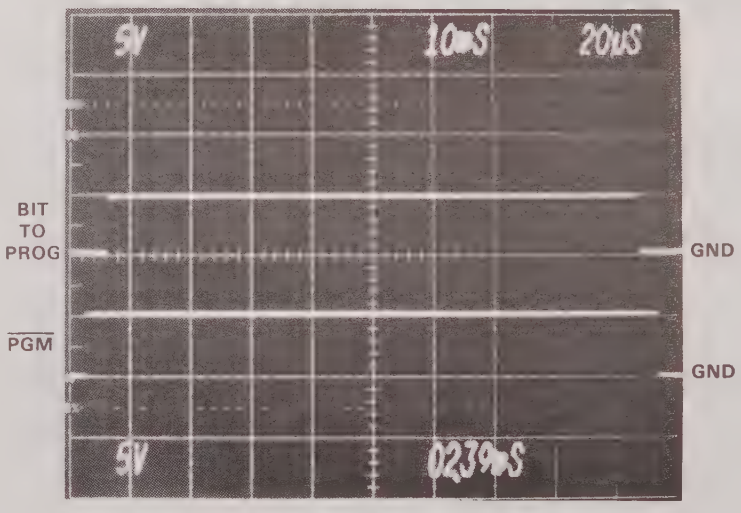
TIMING DIAGRAM

FAMILY CODES 79, 80

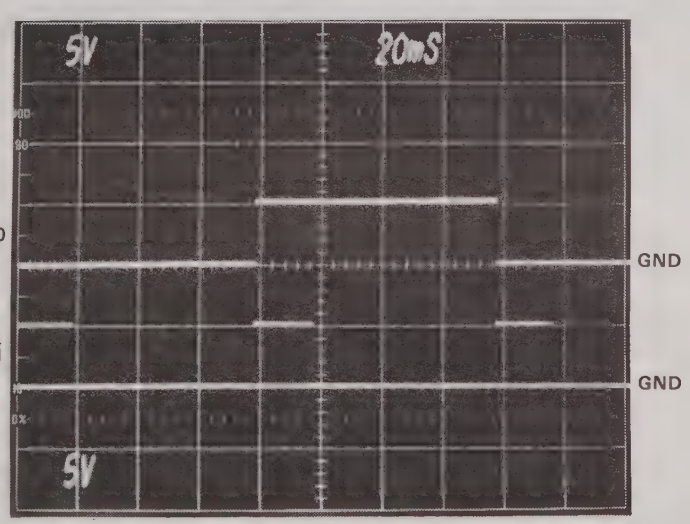
DATA I/O


5V
10mS
BIT
TO
PROG
GND
PGM
GND
5V

5


5V
10mS
20µS
BIT
TO
PROG
GND
PGM
GND
5V

6


5V
20mS
A0
GND
PGM
GND
5V

7

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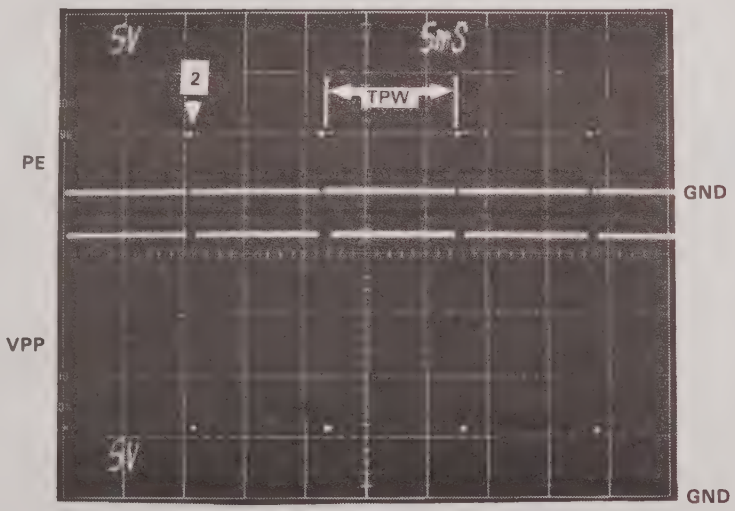
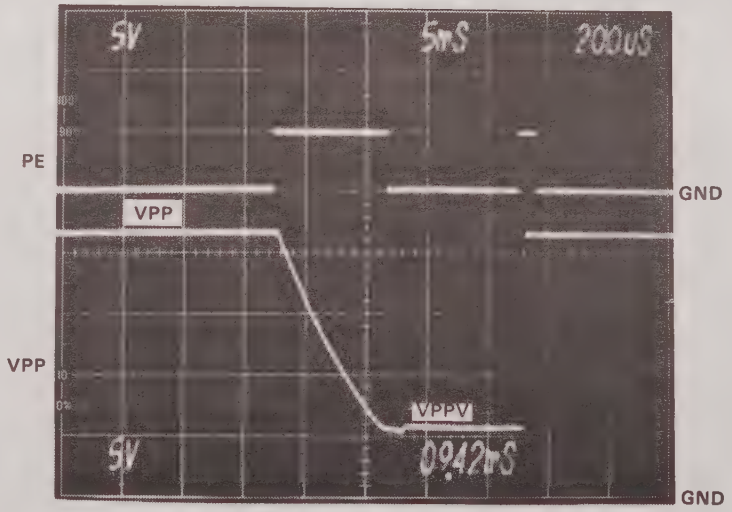
TIMING DIAGRAM

FAMILY CODES 79, 80

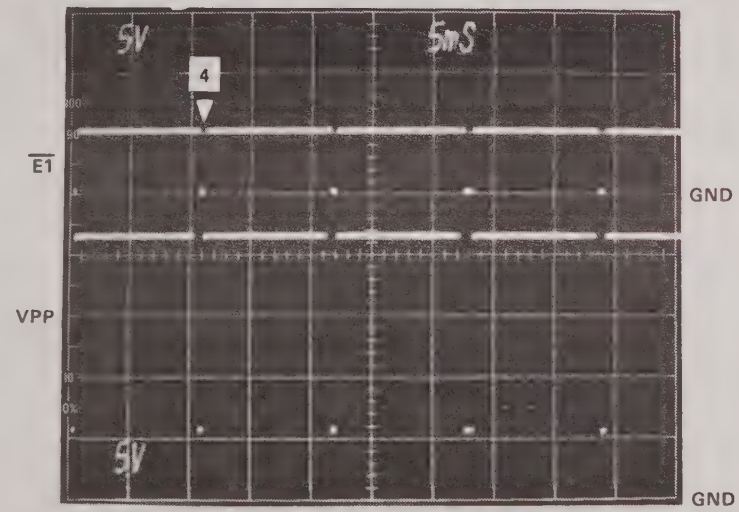
DATA I/O


5V
5mS
2
TPW
PE
GND
VPP
5V
GND

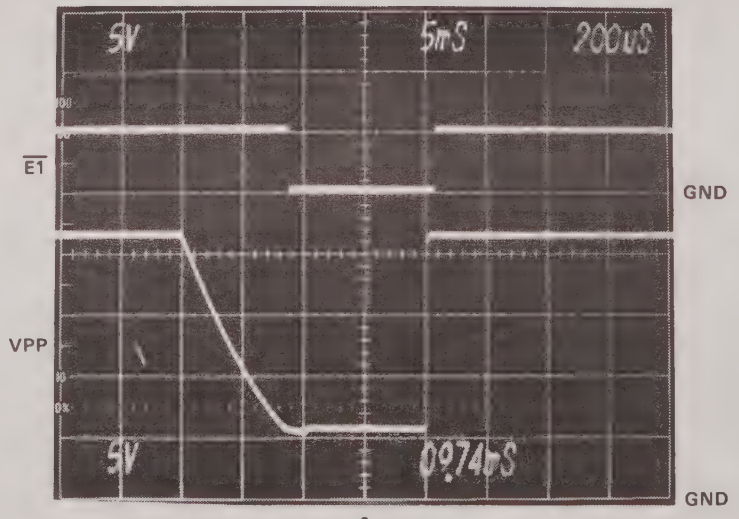
1


5V
5mS
200uS
PE
GND
VPP
VPP
VPPV
5V
0.42mS
GND

2


5V
5mS
4
E1
GND
VPP
5V
GND

3


5V
5mS
200uS
E1
GND
VPP
5V
0.74mS
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	9.8	10.0	10.2	ms	
	TR	1			µs	
	TF	1			µs	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 81.*
2. *Load RAM with hex 01 for Family 82, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 13 through 18 are Byte erase waveforms.*

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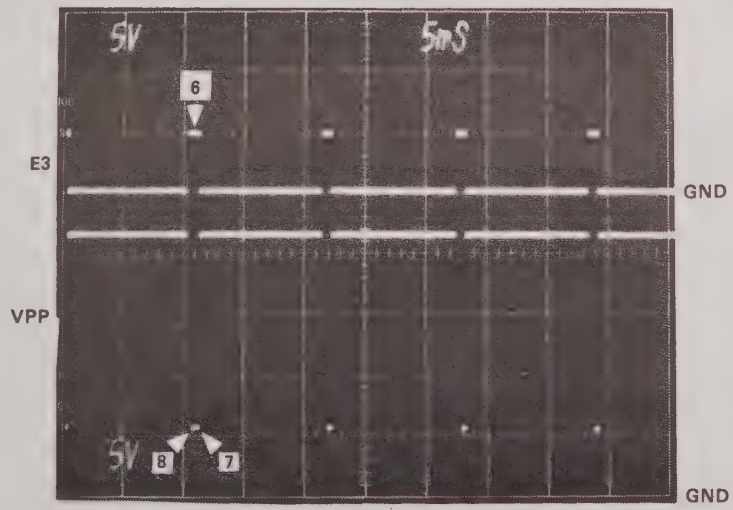
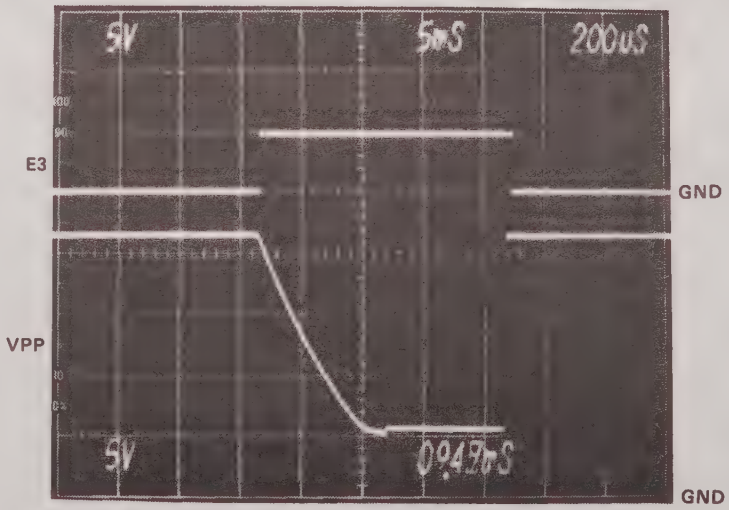
TIMING DIAGRAM

FAMILY CODES 81, 82

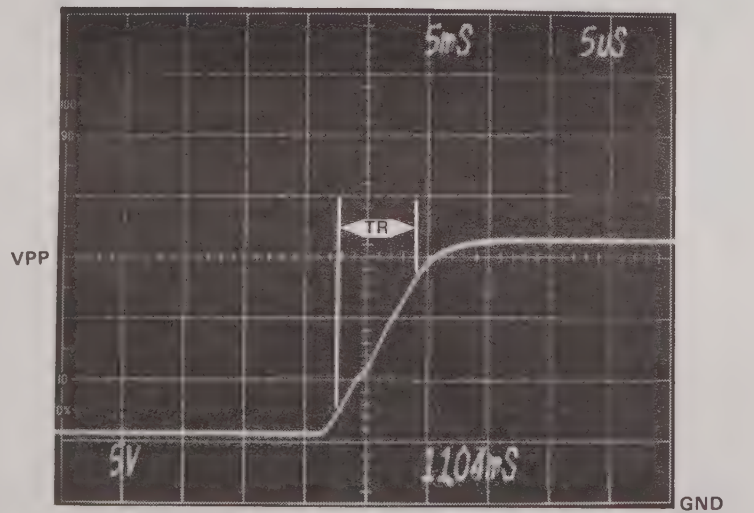
DATA I/O


5V
5mS
6
E3
GND
VPP
5V
8
7
GND

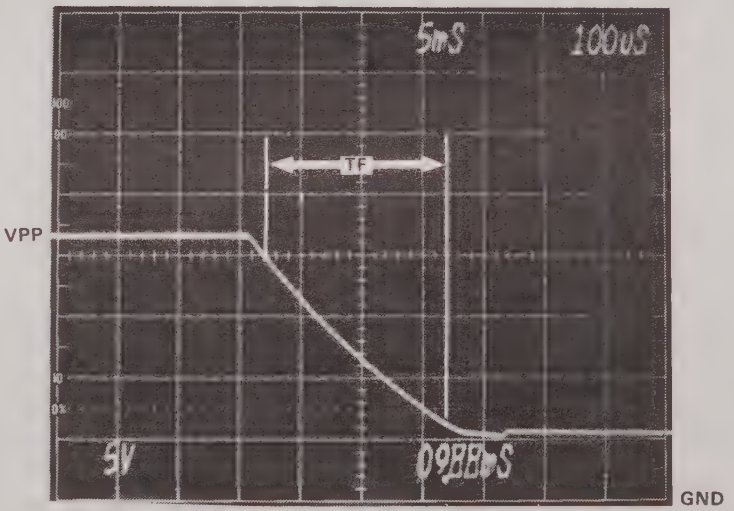
5


5V
5mS
200uS
E3
GND
VPP
5V
GND

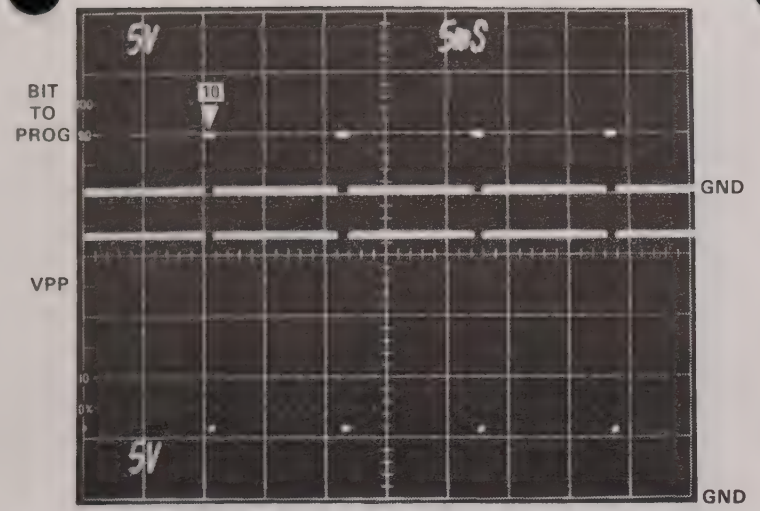
6


5mS
5uS
TR
VPP
5V
GND

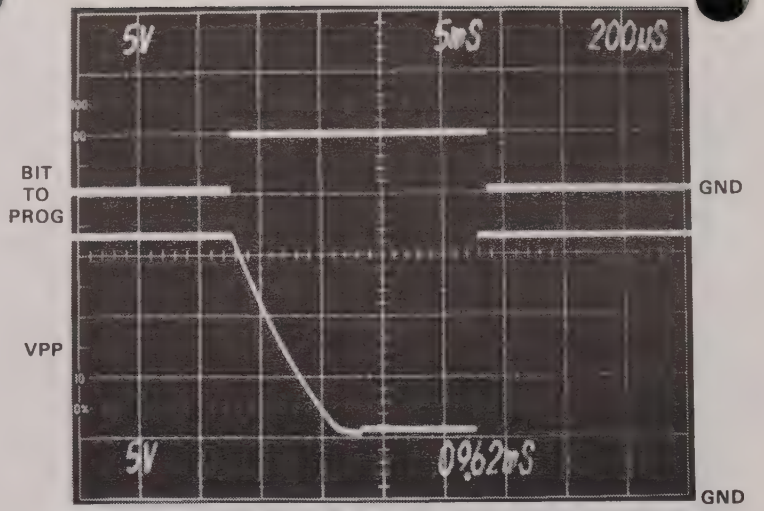
7


5mS
100uS
TF
VPP
5V
GND

8



9



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TIMING DIAGRAM

FAMILY CODES 81, 82

DATA I/O

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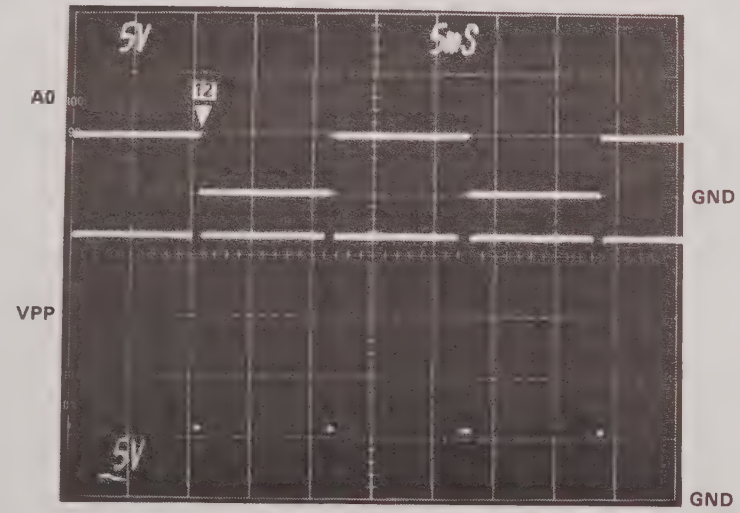
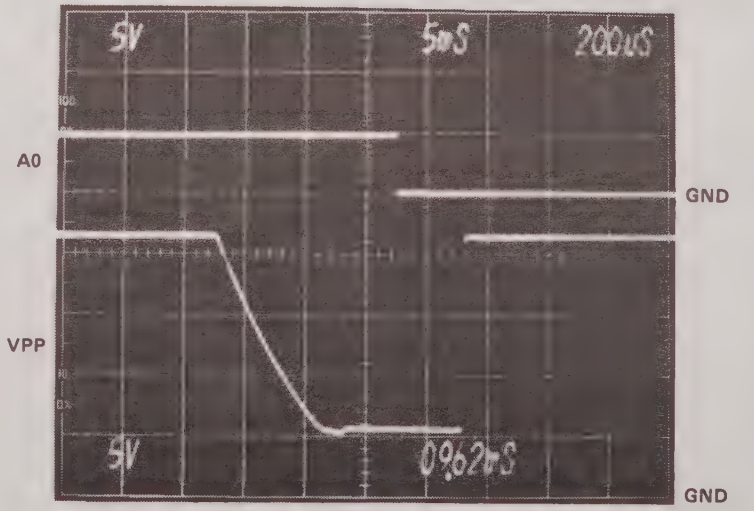
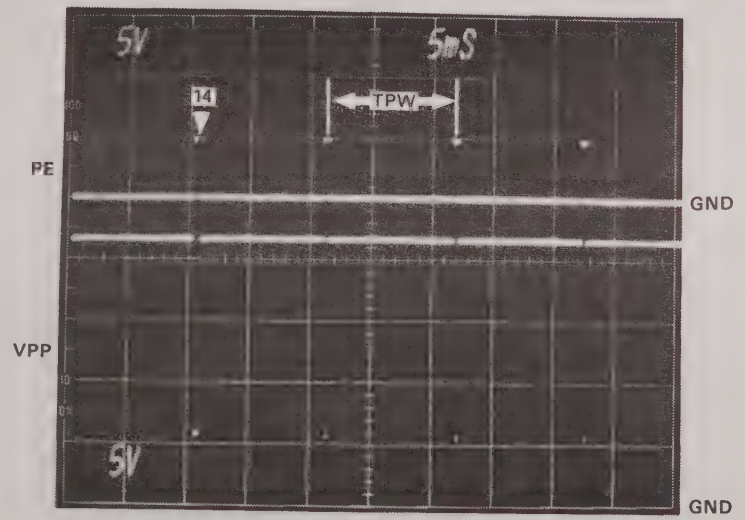

5V
5mS
A0
12
GND
VPP
5V
GND

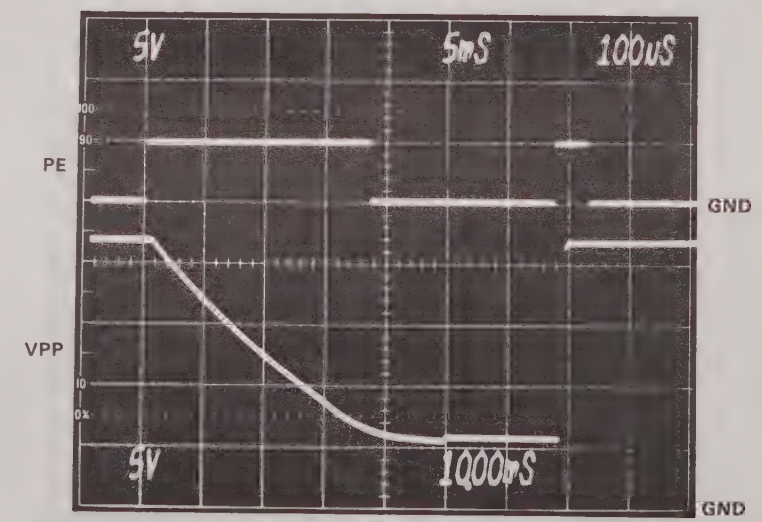
11


5V
5mS
200uS
A0
GND
VPP
5V
0%2mS
GND

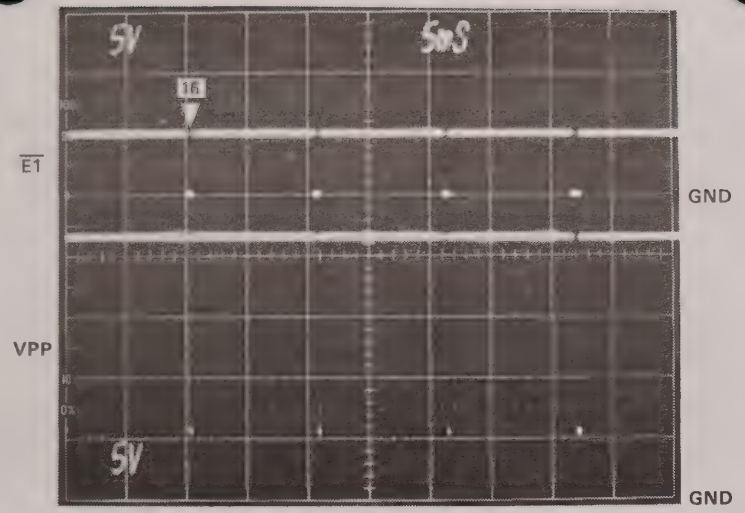
12


5V
5mS
14
TPW
PE
GND
VPP
5V
GND

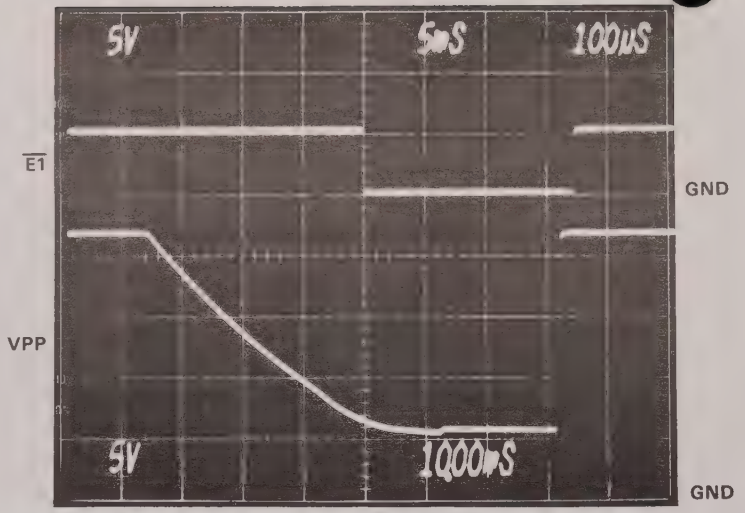
13


5V
5mS
100uS
PE
GND
VPP
5V
1000mS
GND

14



15



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TIMING DIAGRAM

FAMILY CODES 81, 82

DATA I/O

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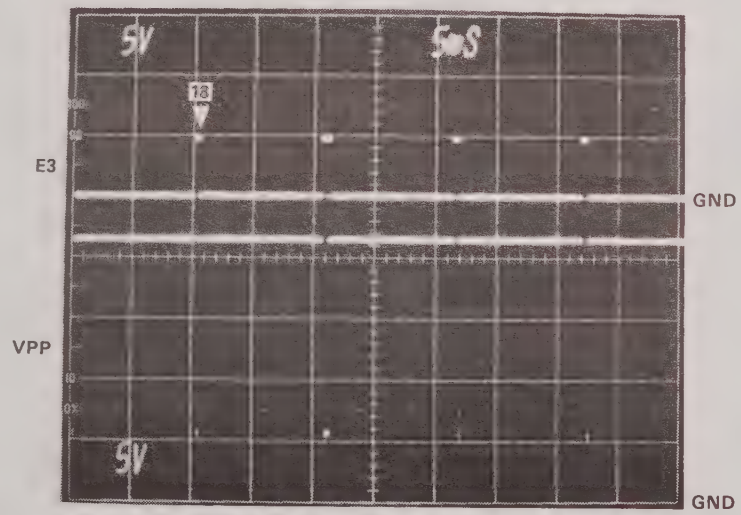
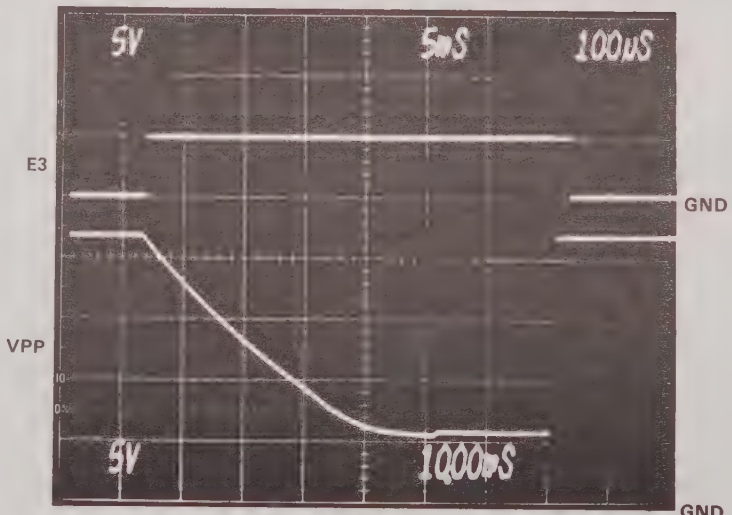


17



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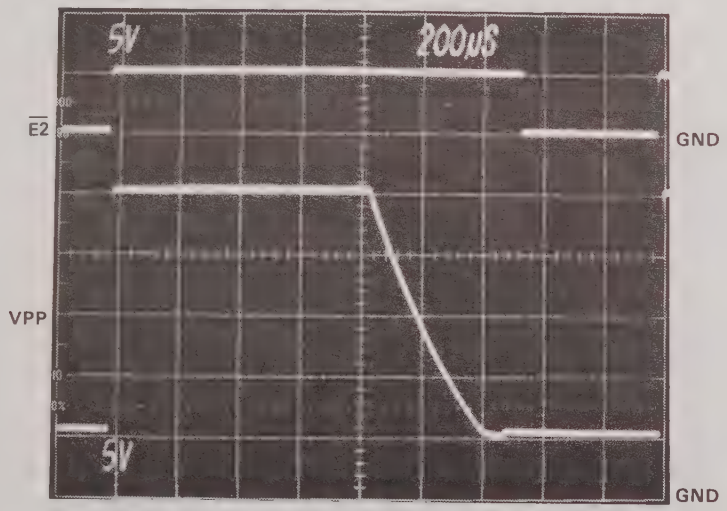
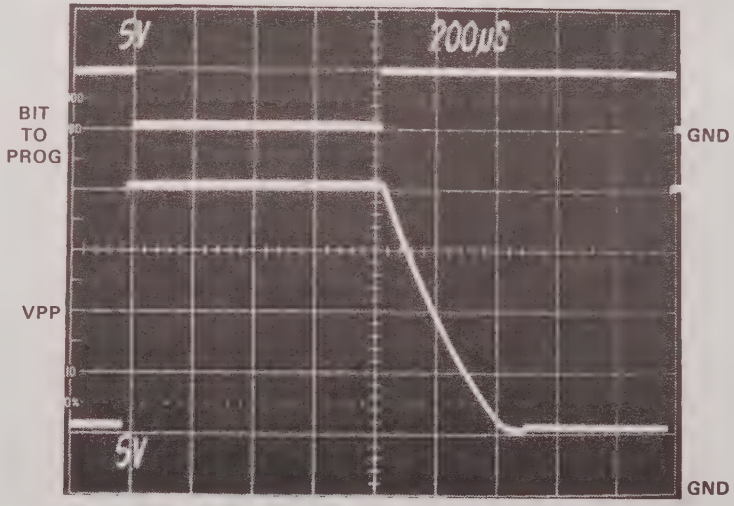
TIMING DIAGRAM

FAMILY CODES 81, 82

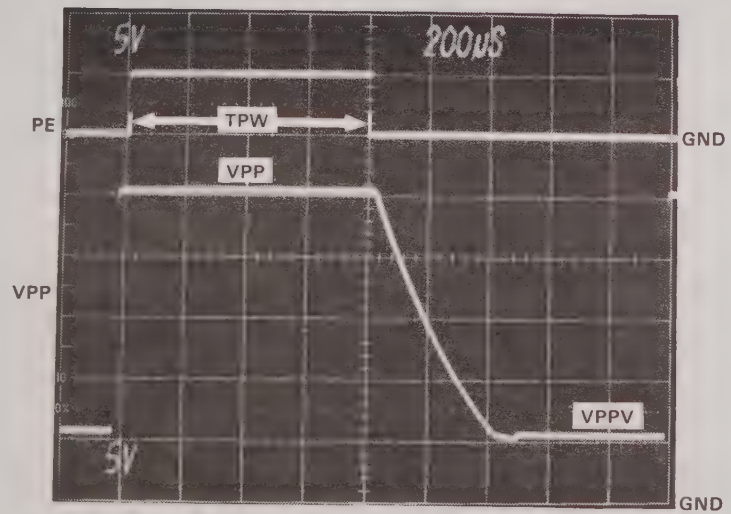
DATA I/O


5V
200uS
$\overline{E2}$
GND
VPP
5V
GND

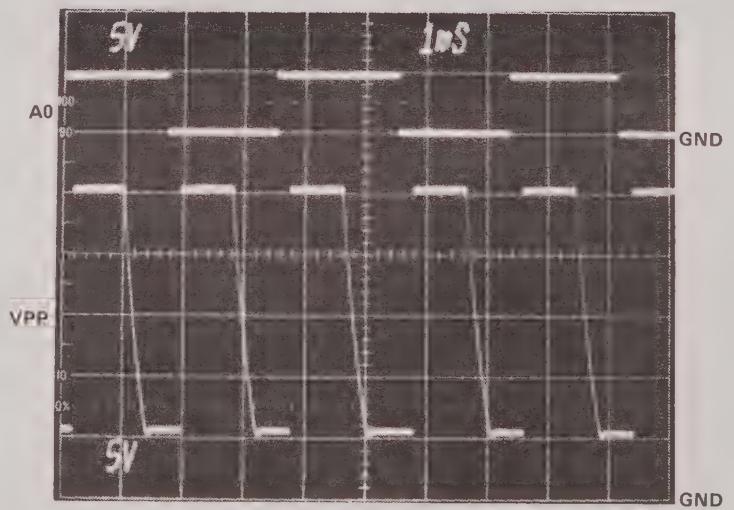
1


5V
200uS
BIT
TO
PROG
GND
VPP
5V
GND

2


5V
200uS
PE
TPW
GND
VPP
VPP
VPPV
5V
GND

3


5V
1mS
A0
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	24.0	25.0	26.0	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	800			µs	
	TR	5			ns	
	TEP	1			sec	
	TF	5			ns	
	Reject		1		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 83.*
2. *Load RAM with hex 01 for Family 84, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photo 7 is the erase waveform.*

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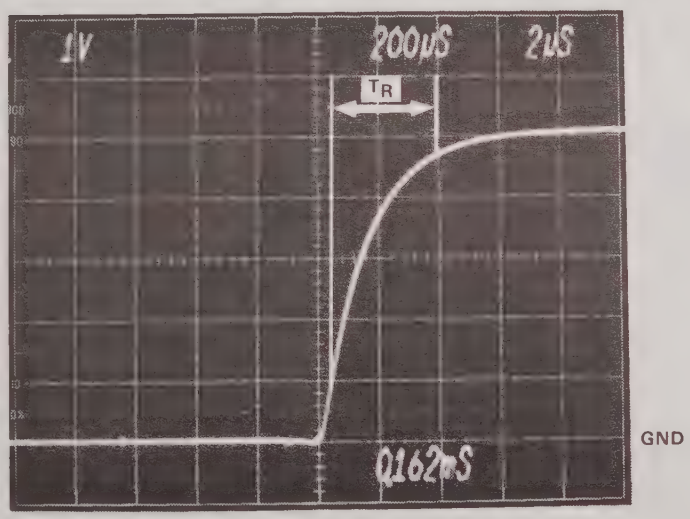
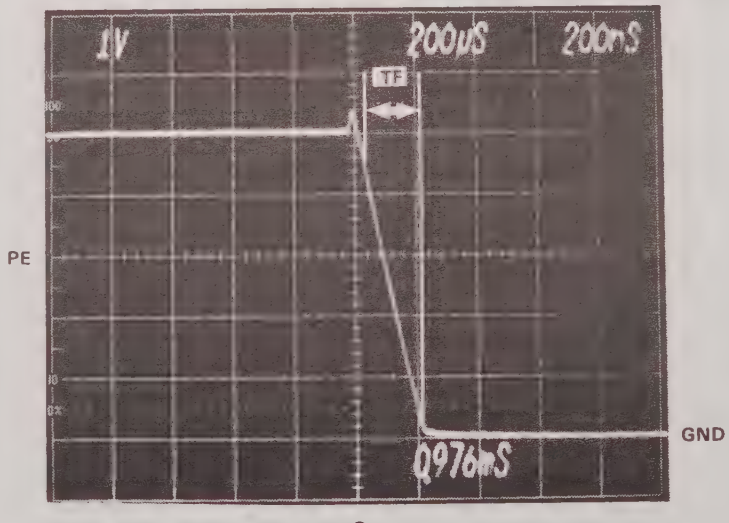
TIMING DIAGRAM

FAMILY CODES 83, 84

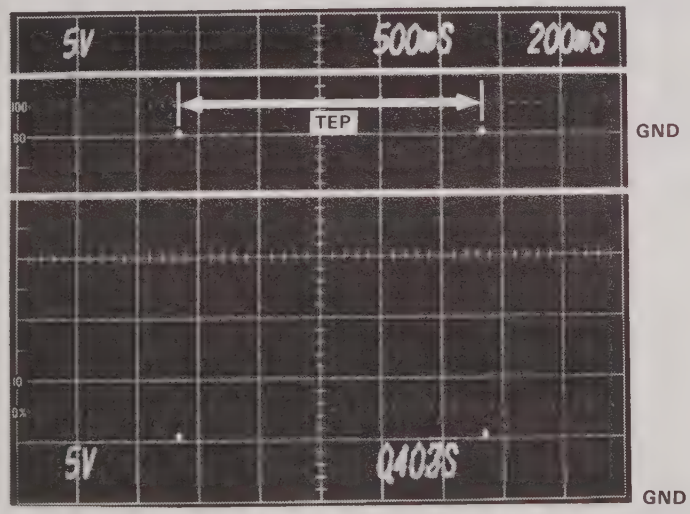
DATA I/O


1V
200µS
2µS
TR
PE
GND
Q162mS

5


1V
200µS
200mS
TF
PE
GND
Q976mS

6


5V
500mS
200mS
PE
TEP
GND
VPP
5V
Q402S
GND

7

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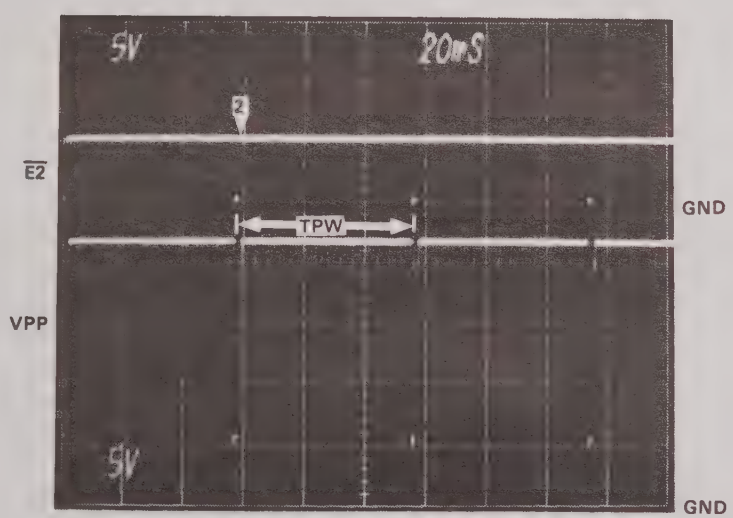
TIMING DIAGRAM

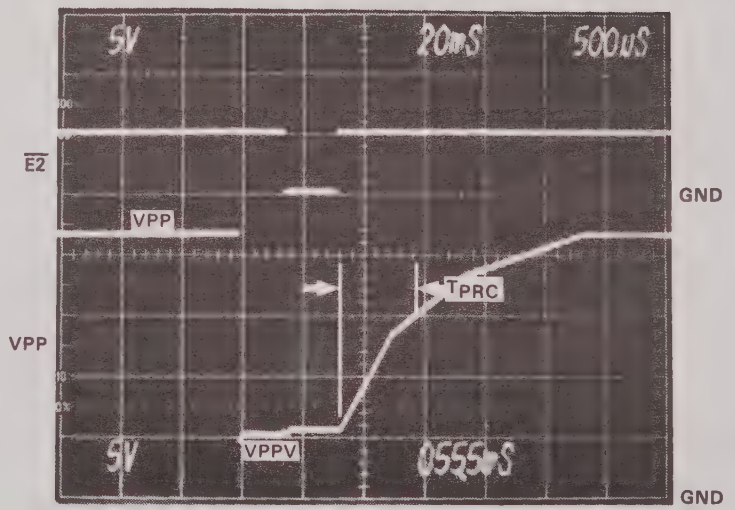
FAMILY CODES 83, 84

DATA I/O

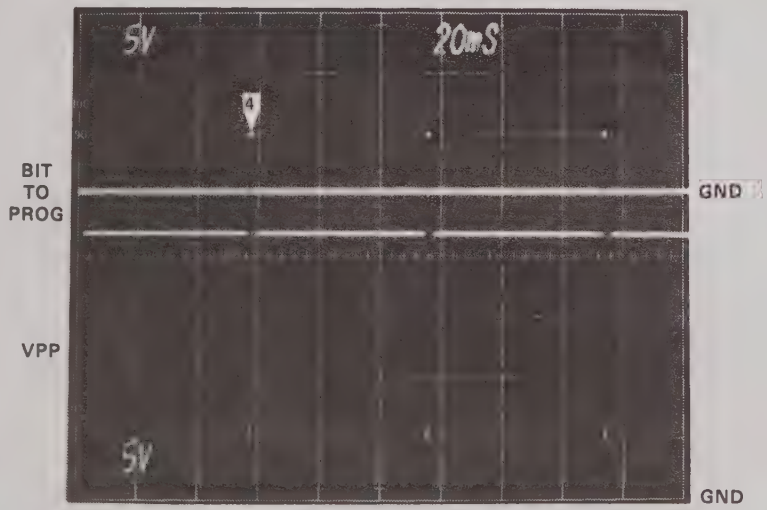
0526/1282


5V
20mS
2
E2
GND
TPW
VPP
5V
GND

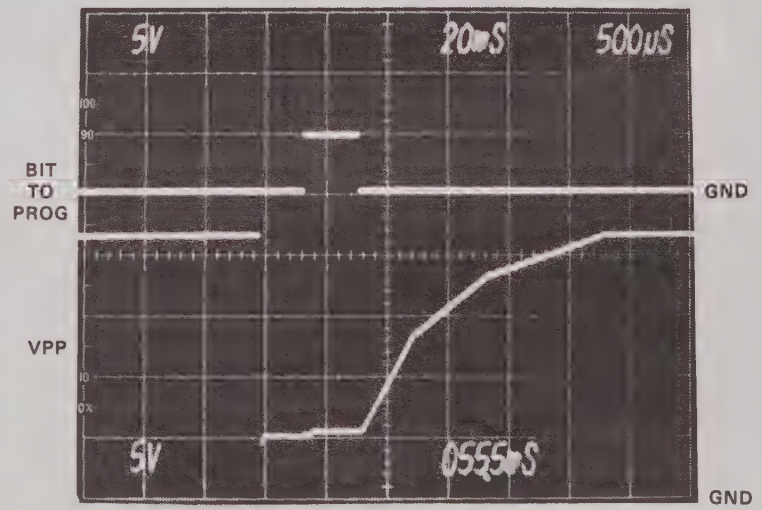
1


5V
20mS
500uS
E2
GND
VPP
TPRC
VPP
5V
VPPV
GND

2


5V
20mS
4
BIT
TO
PROG
GND
VPP
5V
GND

3


5V
20mS
500uS
BIT
TO
PROG
GND
VPP
5V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VOP					NA
	VPP	20.0	21.0	22.0	V	
	VPPV	4.0	5.0	6.0	V	
	VEE	9.0		15.0	V	
	TPW	50		70	ms	
	T_{PRC}	450	600	750	µs	See note 3
	T_F			100	µs	
	Reject		2		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

1. Load RAM with hex FE for Family 85.
2. Load RAM with hex 01 for Family 86, and bit-to-prog waveform becomes bit-no-prog.
3. TPRC is measured from 6V to 15.5V.
4. Photos 8 and 9 are erase waveforms.

REVISIONS

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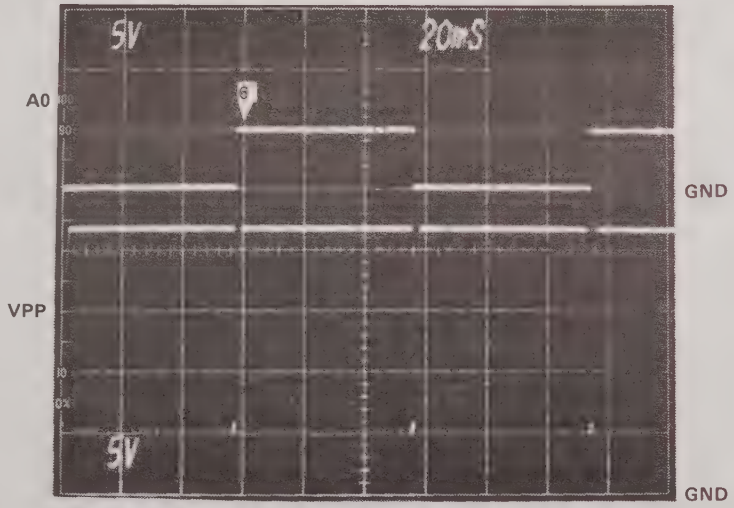
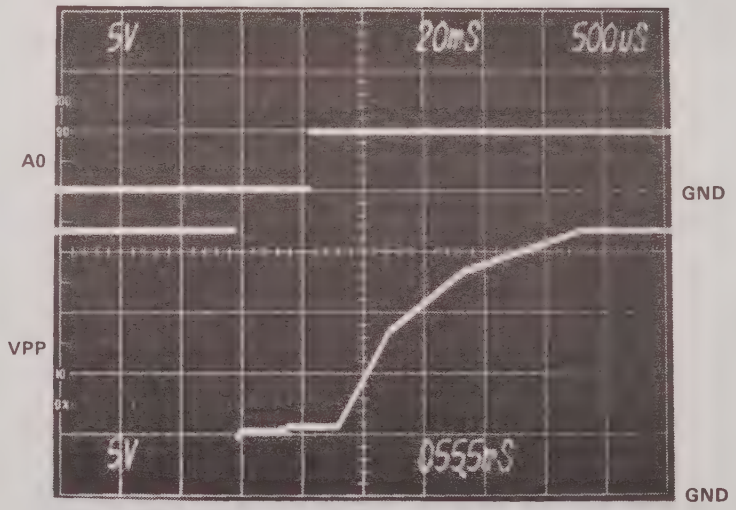
TIMING DIAGRAM

FAMILY CODES 85, 86

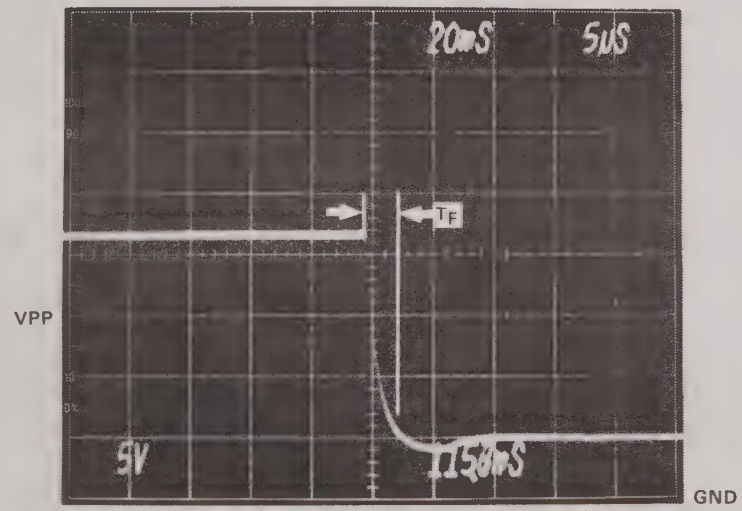
DATA I/O


5V
20mS
A0
GND
VPP
5V
GND

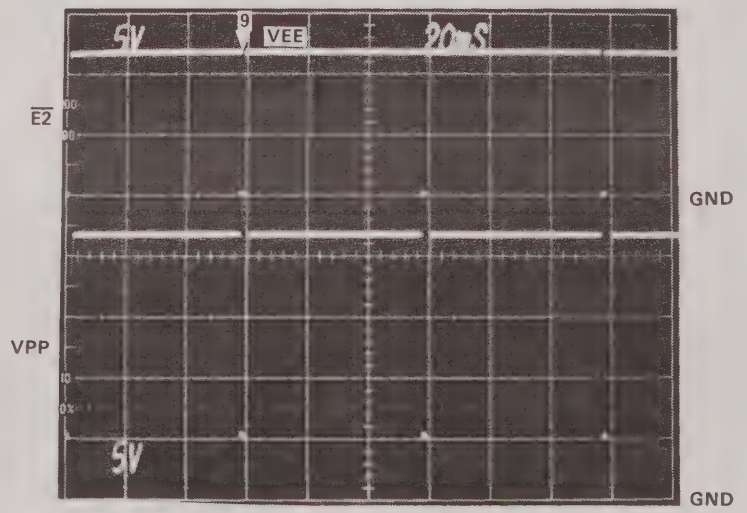
5


5V
20mS
500uS
A0
GND
VPP
5V
GND

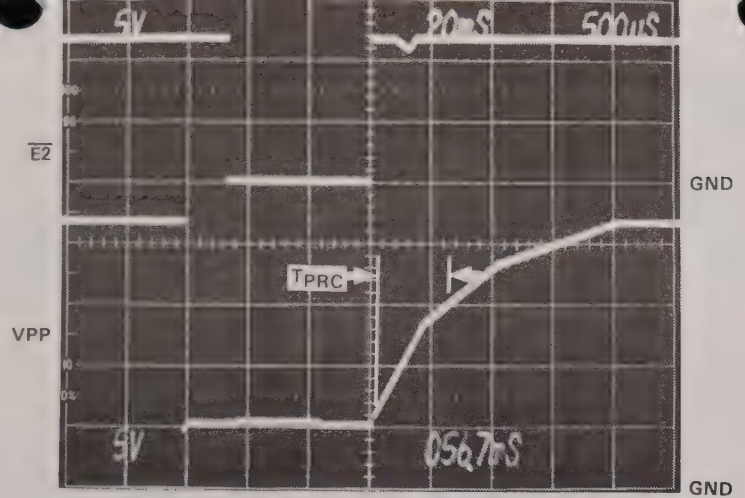
6


20mS
5uS
VPP
5V
GND

7


5V
VEE
20mS
E2
GND
VPP
5V
GND

8



9

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	ECN #5022	CTZ	3/84

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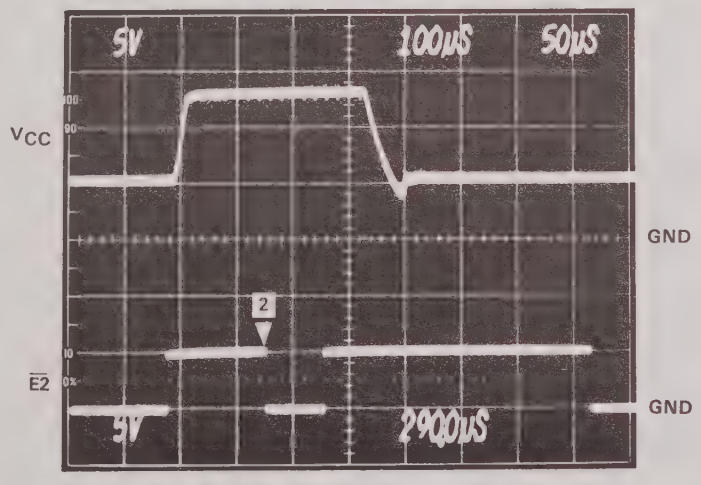
TIMING DIAGRAM

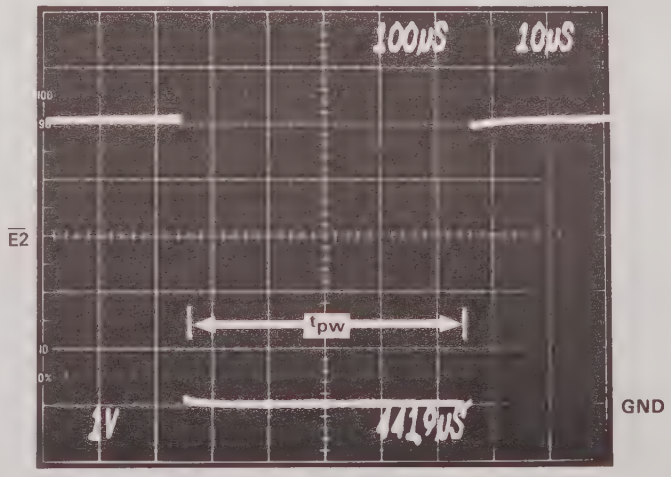
FAMILY CODES 85, 86

DATA I/O

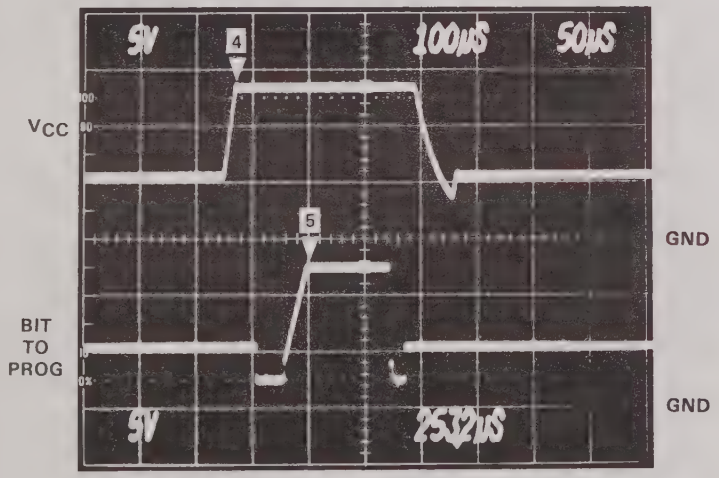
0526/1282


5V
100µS
50µS
VCC
GND
2
E2
GND
5V
2900µS

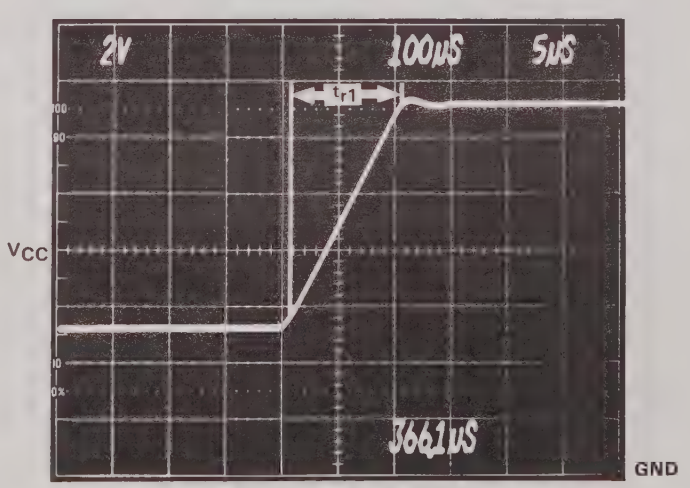
1


100µS
10µS
E2
tpw
GND
1V
1719µS

2


5V
4
100µS
50µS
VCC
GND
5
BIT
TO
PROG
GND
5V
2532µS

3


2V
100µS
5µS
tr1
VCC
GND
3661µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	12.5	12.5	13.0	V	
	V_{OP}	11.5	12.0	12.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{CCN}	4.75	5.0	5.25	V	
	t_{pw}	40	50	60	μs	
	t_{r1}	5		20	μs	
	t_{r2}	10		20	μs	
	Reject		1		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.4	0.5	0.6	V	701-1998/TP4
	HIGH LOAD	16.9	17.9	18.9	V	701-1998/TP2
	LOW LOAD	16.9	17.9	18.9	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	22.1	23.1	24.1	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 91.*
2. *Load RAM with hex 01 for Family 92.*

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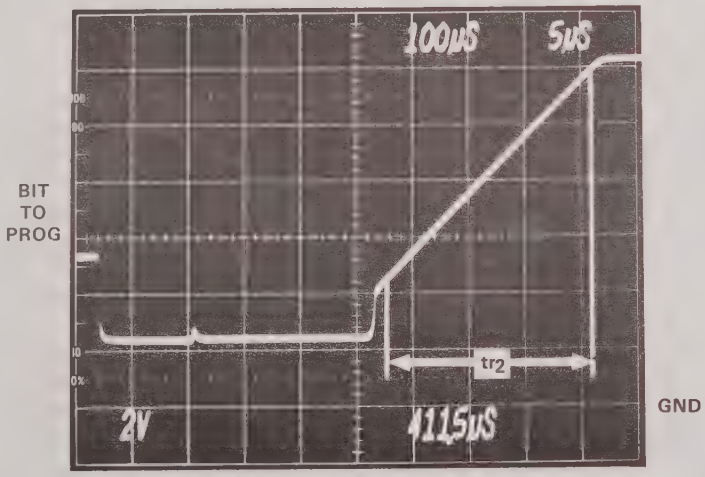
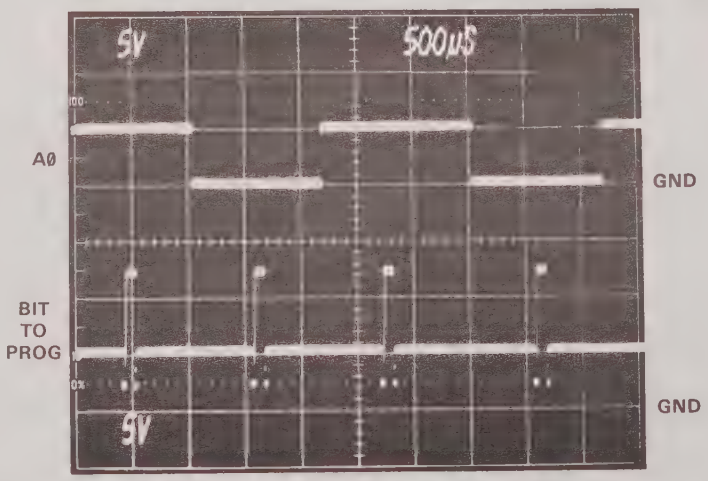
TIMING DIAGRAM

FAMILY CODES 91, 92

DATA I/O


100µS
5µS
BIT
TO
PROG
tr2
GND
2V
1115µS

5


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

6

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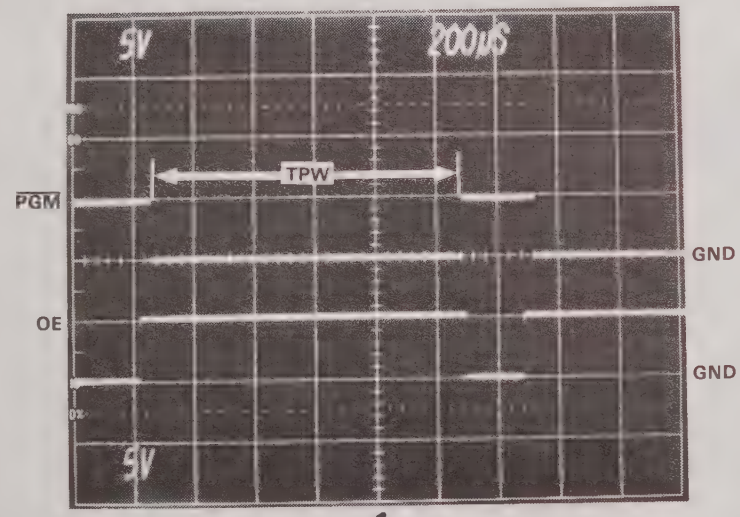
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

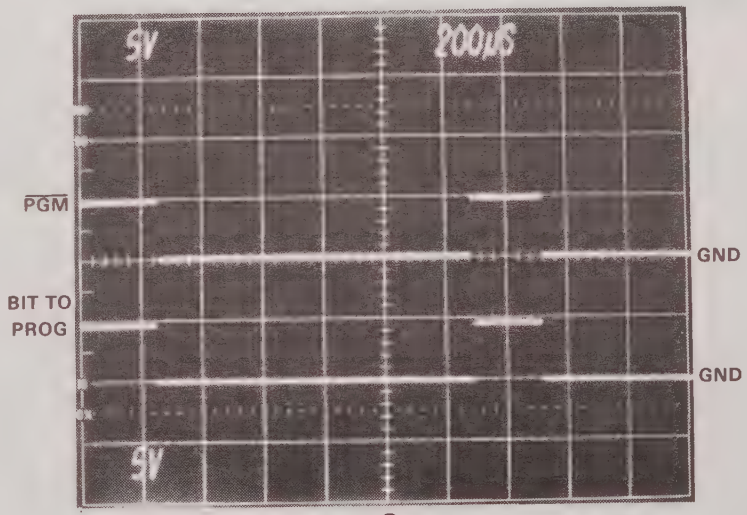
TIMING DIAGRAM

FAMILY CODES 91, 92

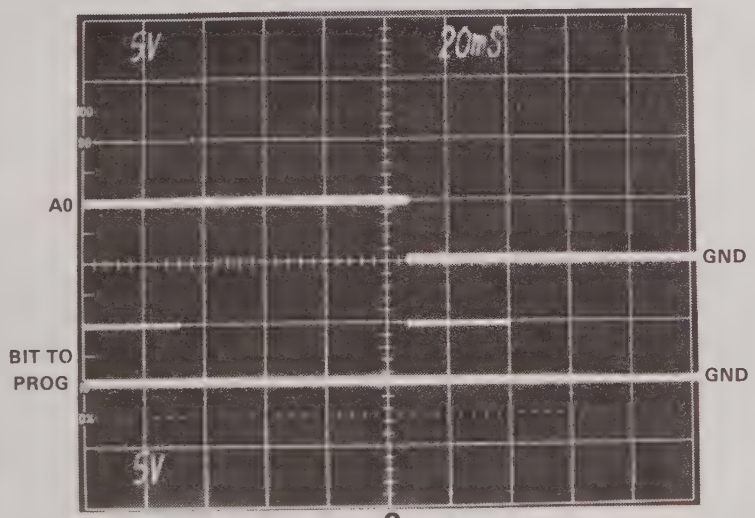
DATA I/O


5V
200µS
TPW
PGM
GND
OE
GND
5V

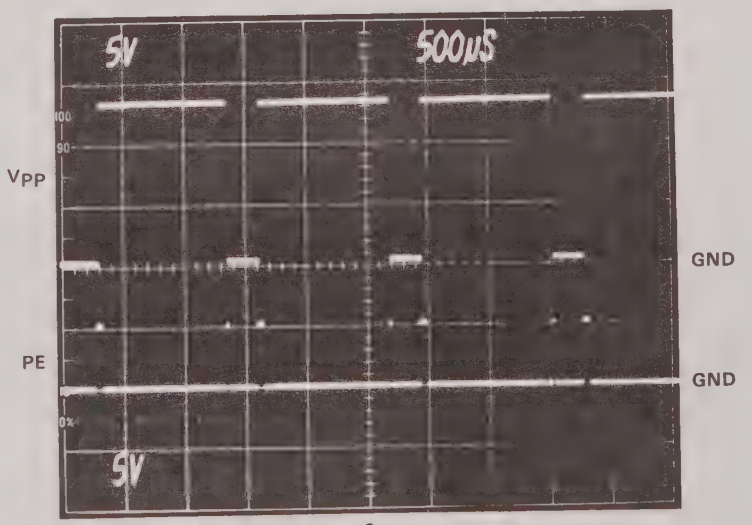
1


5V
200µS
PGM
GND
BIT TO
PROG
GND
5V

2


5V
20mS
A0
GND
BIT TO
PROG
GND
5V

3


5V
500µS
VPP
GND
PE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.75	6.00	6.25	V	Not shown
	VOP					NA
	VPP	12.2	12.5	12.8	V	Not shown
	VPPV					NA
	TPW	0.95	1.0	1.05	ms	
	TR					NA
	TF					NA
	Reject		25		Pulses	
	Overprogram		1		Pulse	See note 3
2ND PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
1ST PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 93.*
2. *Load RAM with hex 01 for Family 94, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 3 ms times the number of programming pulses required to program the location.*
4. *Photo 4 is for Pinout 24.*

REVISIONS

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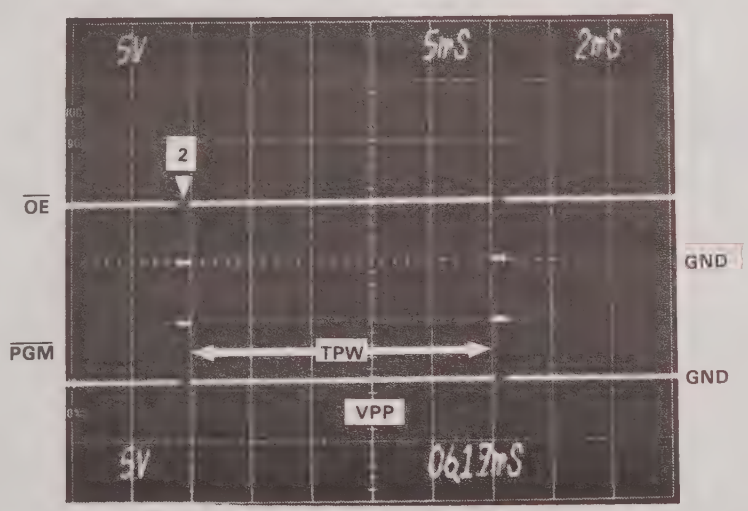
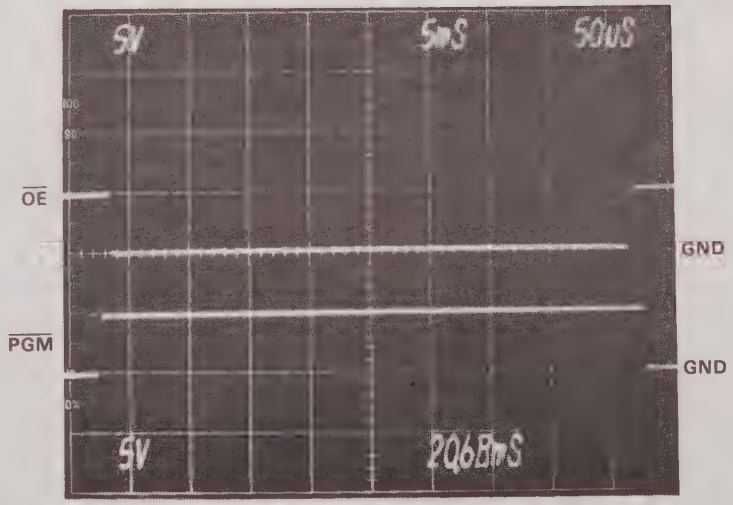
TIMING DIAGRAM

FAMILY CODES 93, 94

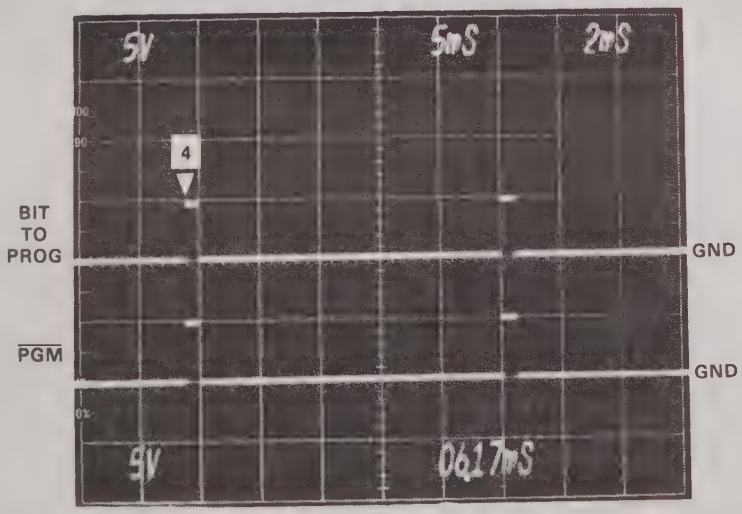
DATA I/O


5V
5mS
2mS
2
OE
GND
PGM
TPW
GND
VPP
5V
0617mS

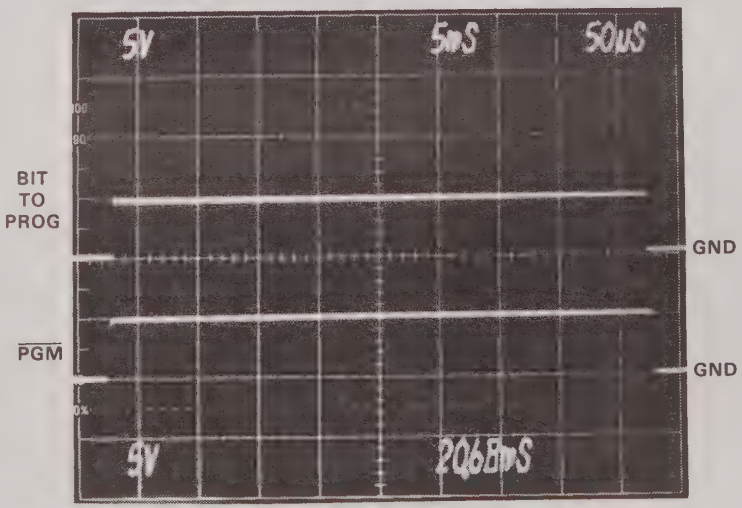
1


5V
5mS
50uS
OE
GND
PGM
GND
5V
2068mS

2


5V
5mS
2mS
4
BIT
TO
PROG
GND
PGM
GND
5V
0617mS

3


5V
5mS
50uS
BIT
TO
PROG
GND
PGM
GND
5V
2068mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.5	5.0	5.5	V	
	VPP	0.0	0.0	0.8	V	
	VEE	12.0	14.5	21.0	V	
	TPW	5.0	10.0	15.0	ms	
	TR				NA	
	TF				NA	
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.9	7.9	8.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family A5.*
2. *Load RAM with hex 01 for Family A6, and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Photos 6 and 7 are erase waveforms.*

REVISIONS

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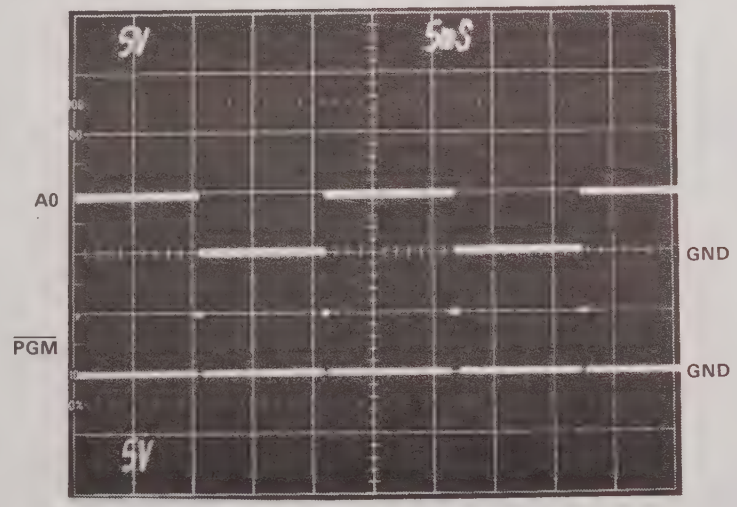
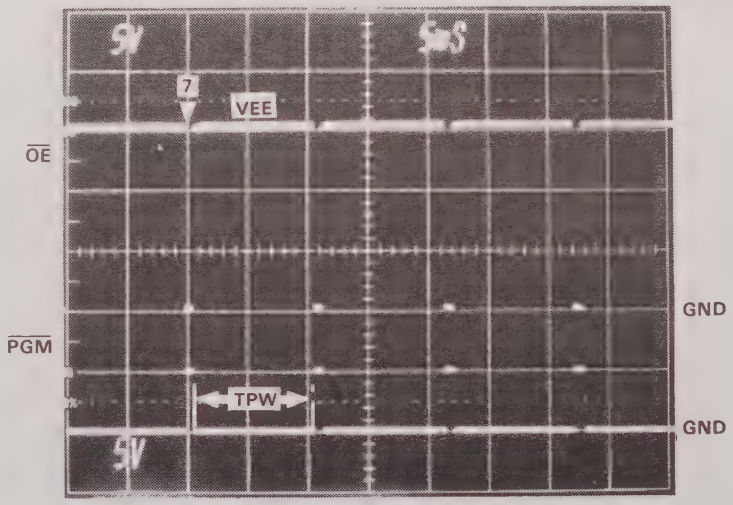
TIMING DIAGRAM

FAMILY CODES A5, A6

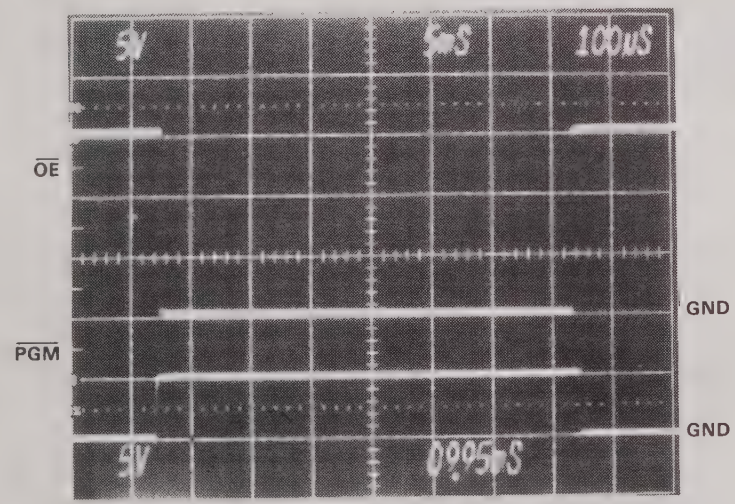
DATA I/O


5V
5mS
A0
GND
PGM
GND
5V

5


5V
5mS
7
VEE
OE
GND
PGM
TPW
GND
5V

6


5V
5mS
100uS
OE
GND
PGM
GND
5V
0.05mS

7

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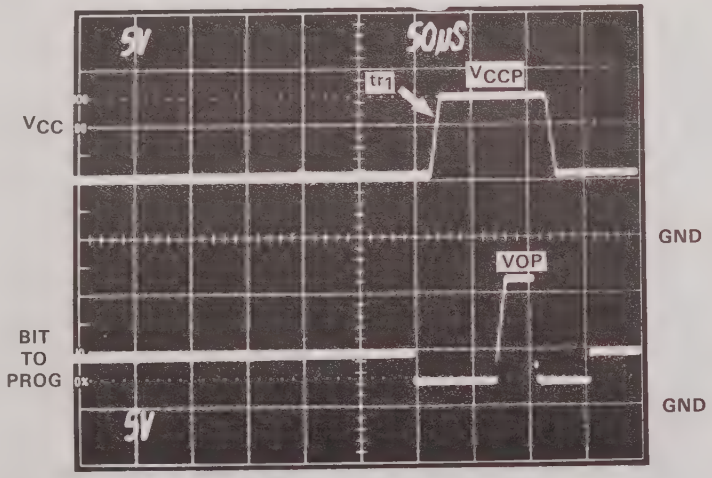
TIMING DIAGRAM

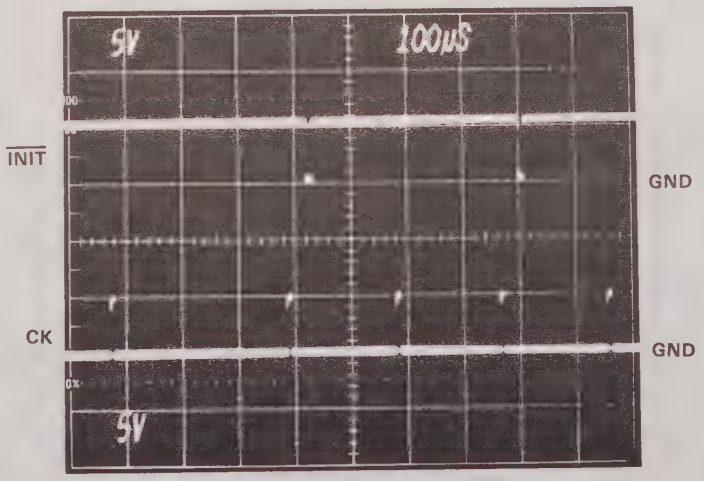
FAMILY CODES A5, A6

DATA I/O

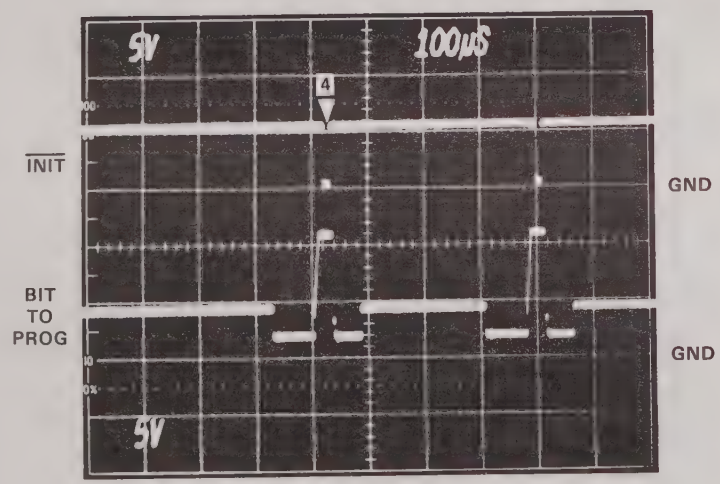
0526/1282


5V
50µS
tr1
VCCP
VCC
GND
VOP
BIT
TO
PROG
GND
5V

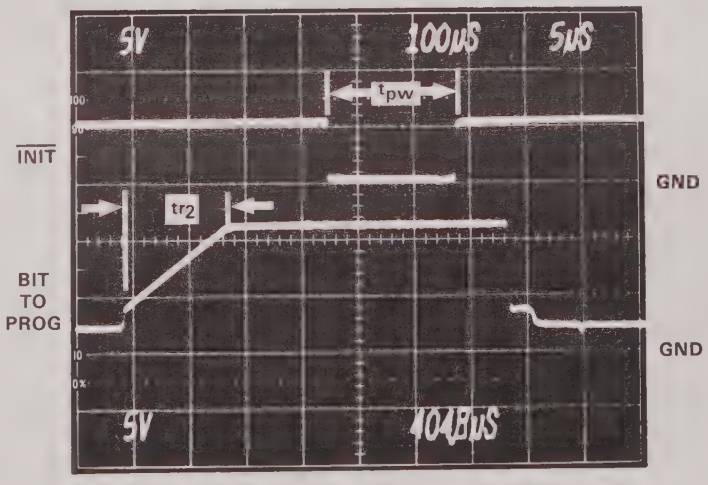
1


5V
100µS
INIT
GND
CK
GND
5V

2


5V
100µS
4
INIT
GND
BIT
TO
PROG
GND
5V

3


5V
100µS
5µS
tpw
INIT
GND
tr2
BIT
TO
PROG
GND
5V
10µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	11.6	11.8	12.0	V	
	V_{OP}	10.5	11.0	11.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.0	10.0	11.5	μs	
	t_{r1}	1		20.0	μs	See note 3.
	t_{r2}	1		15.0	μs	
	Reject		10		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	3.4	3.5	3.6	V	701-1998/TP4
	HIGH LOAD	7.7	8.7	9.7	V	701-1998/TP2
	LOW LOAD	7.7	8.7	9.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family A9.*
2. *Load RAM with hex 01 for Family AA.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

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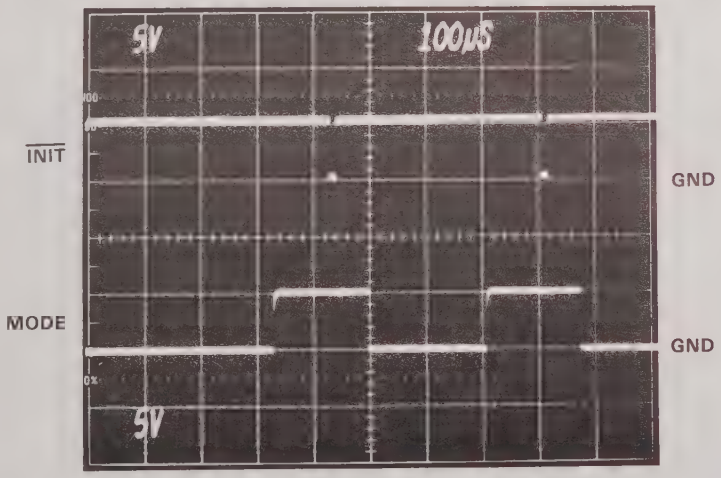
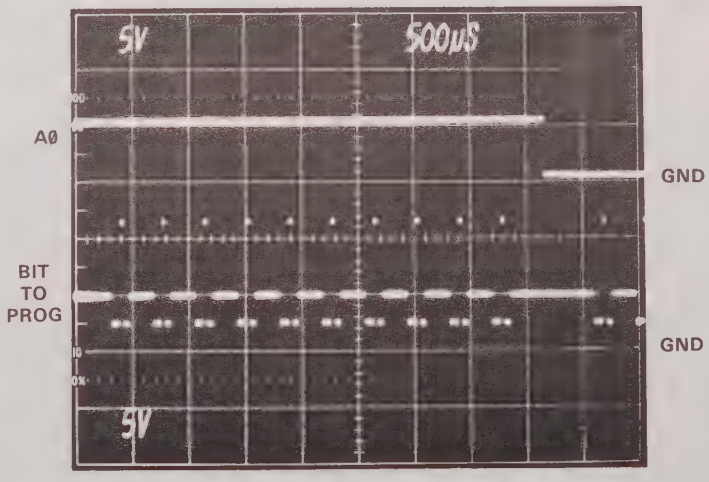
TIMING DIAGRAM

FAMILY CODES A9, AA

DATA I/O



5



6

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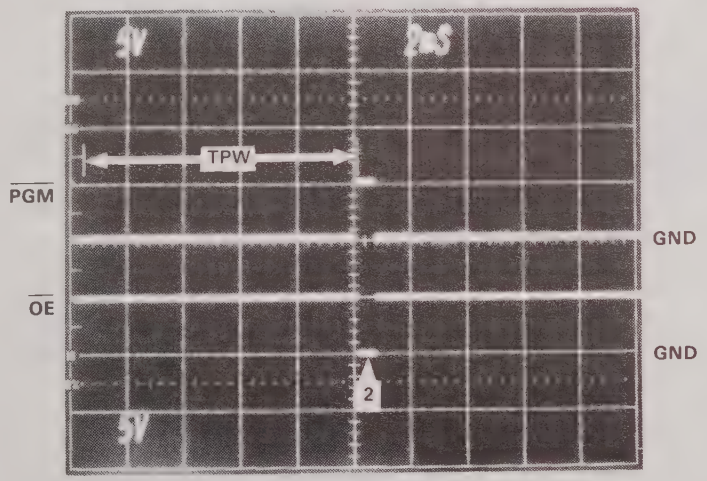
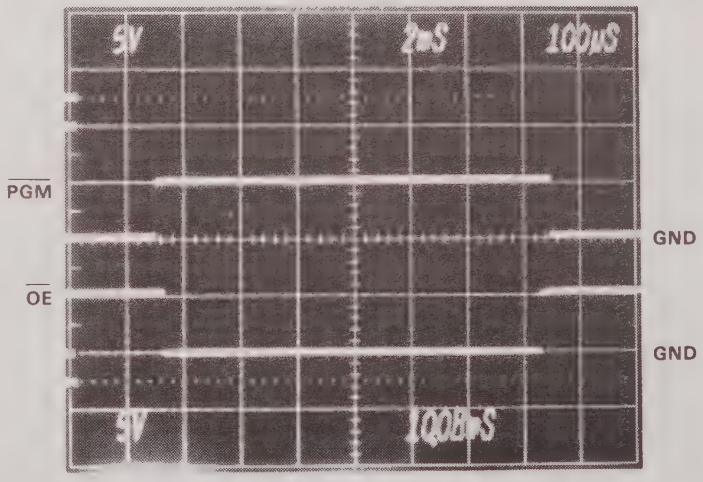
TIMING DIAGRAM

FAMILY CODES A9, AA

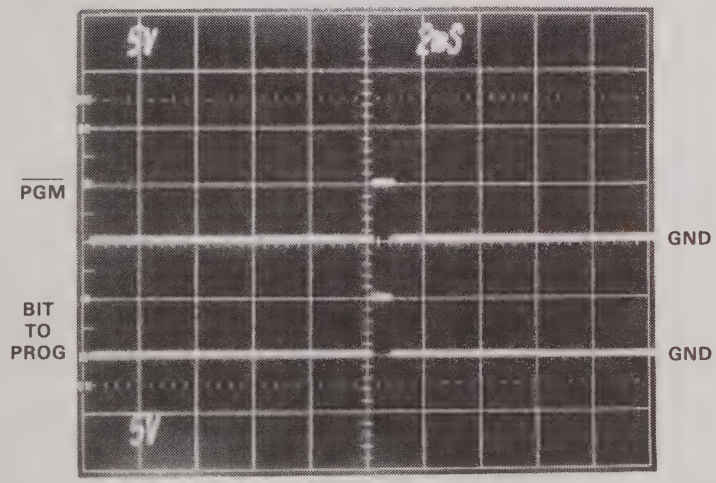
DATA I/O


5V
2mS
TPW
PGM
GND
OE
GND
2
5V

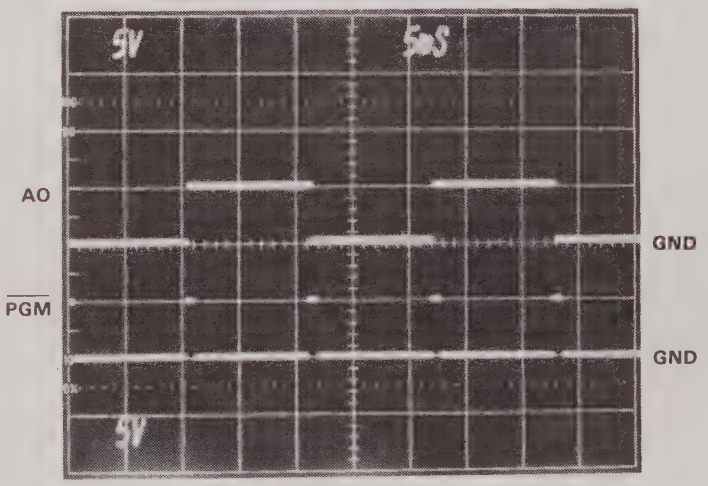
1


5V
2mS
100μS
PGM
GND
OE
GND
5V
100μS

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
5mS
AO
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family AB.*
2. *Photos 5 to 8 are chip erase waveforms.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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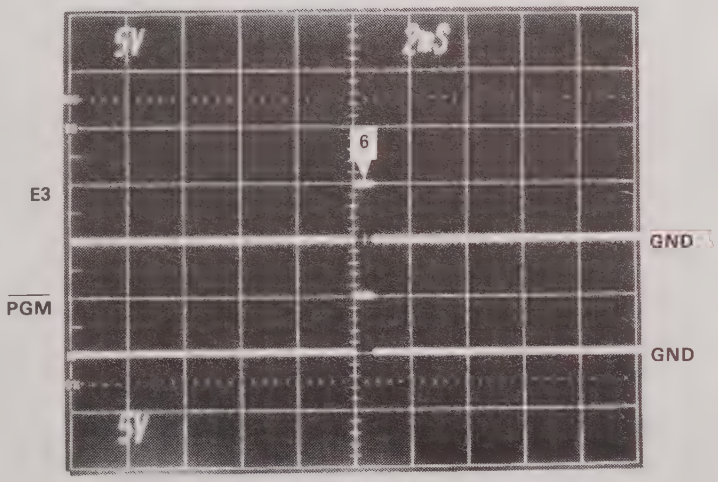
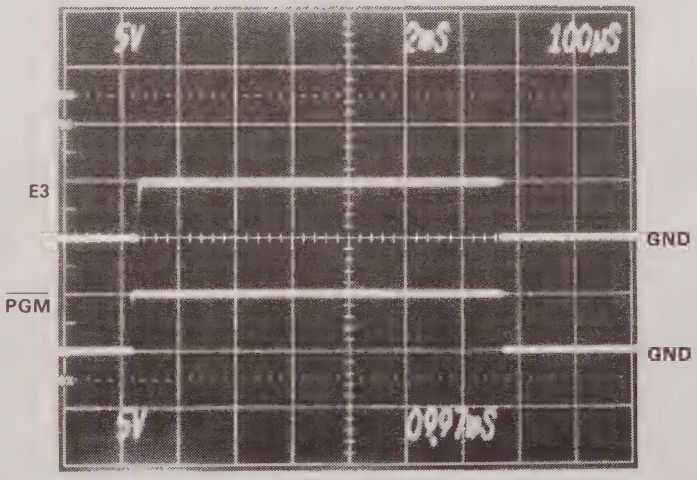
TIMING DIAGRAM

FAMILY CODES AB, AC

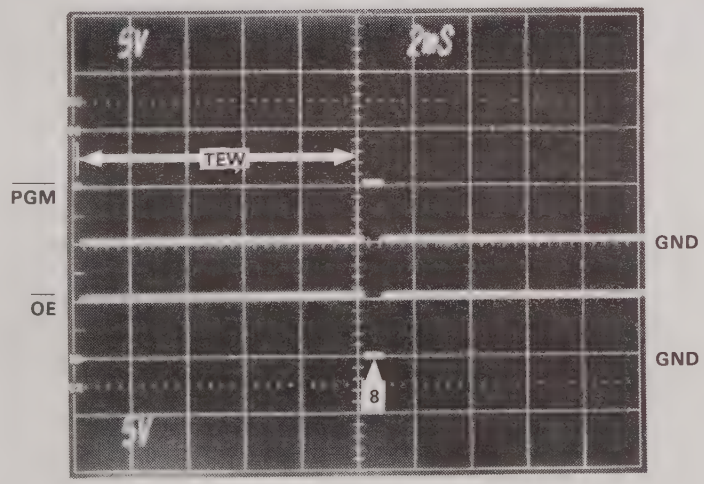
DATA I/O


5V
2mS
6
E3
GND
PGM
GND
5V

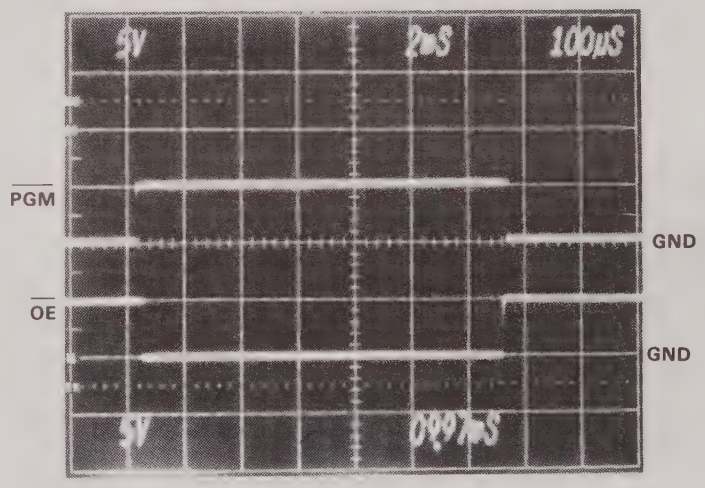
5


5V
2mS
100uS
E3
GND
PGM
GND
5V

6


5V
2mS
TEW
PGM
GND
OE
GND
8
5V

7


5V
2mS
100uS
PGM
GND
OE
GND
5V

8

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	ECN #5022	CTZ	3/84

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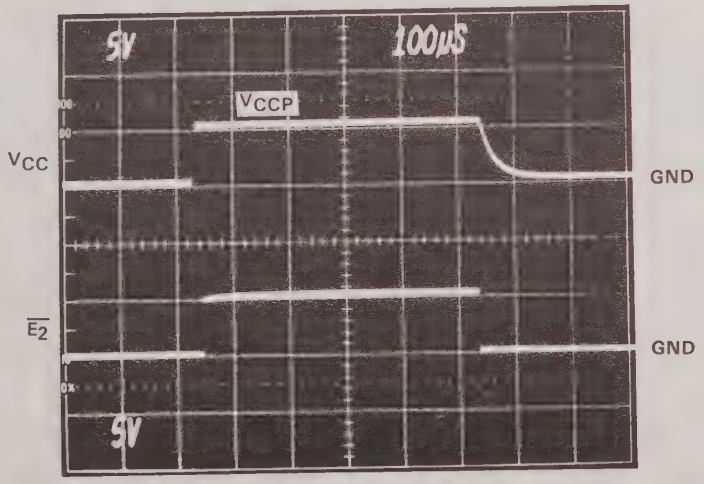
TIMING DIAGRAM

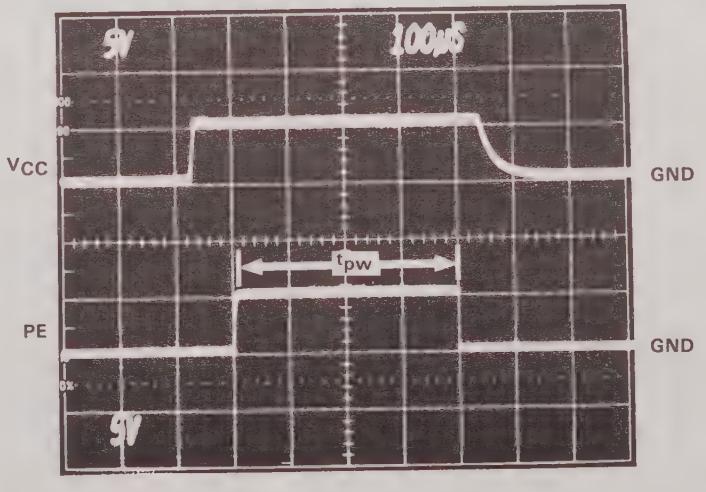
FAMILY CODES AB, AC

DATA I/O

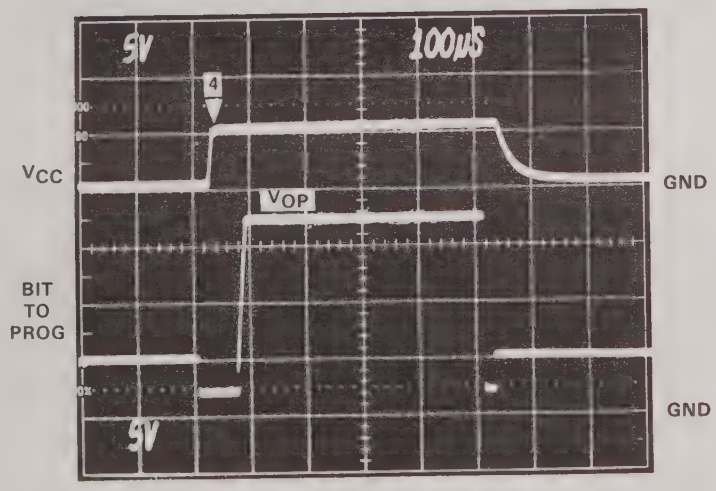
0526/1282


5V
100µS
VCCP
VCC
GND
E2
GND
5V

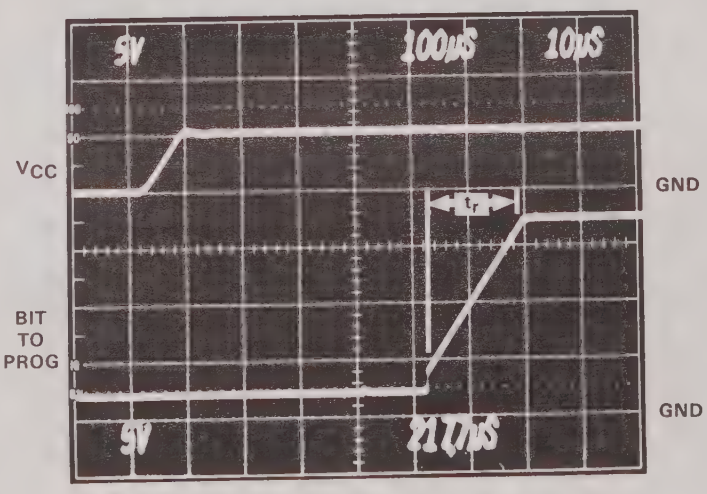
1


5V
100µS
VCC
GND
tpw
PE
GND
5V

2


5V
100µS
4
VCC
GND
VOP
BIT
TO
PROG
GND
5V

3


5V
100µS
10µS
VCC
GND
tr
BIT
TO
PROG
GND
5V
21.7µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	
	V_{OP}	16.0	17.0	18.0	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	300	400	500	μs	
	t_r	10		50	μs	
	Reject		1		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	1.4	1.5	1.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.7	5.2	5.7	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.4	1.5	1.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.7	5.2	5.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family AD.*
2. *Load RAM with hex 01 for Family AE.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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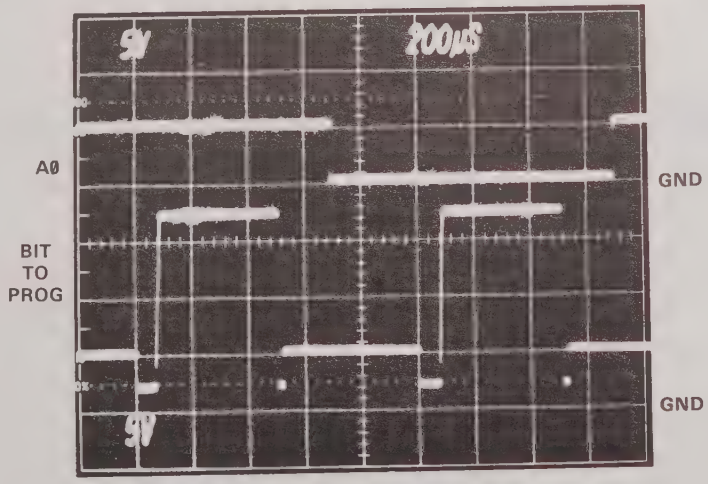
TIMING DIAGRAM

FAMILY CODES AD, AE

DATA I/O



5

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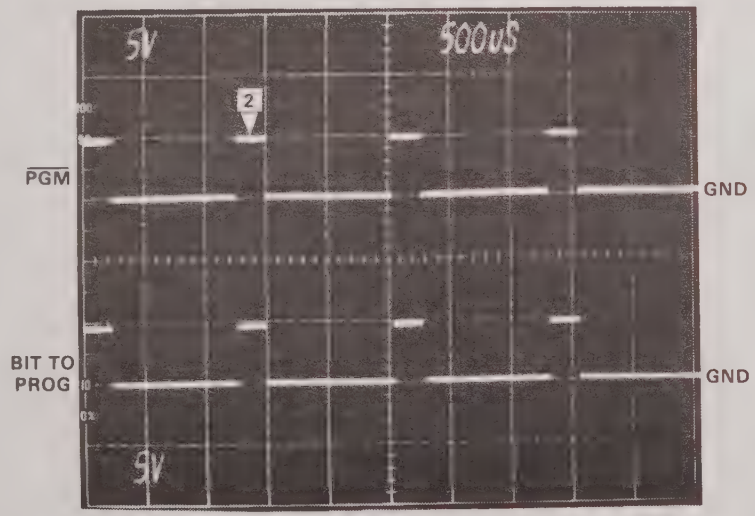
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022		

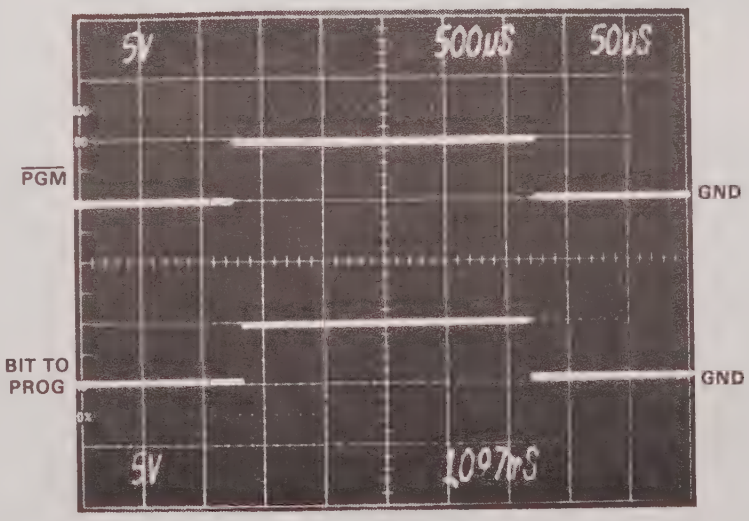
TIMING DIAGRAM

FAMILY CODES AD, AE

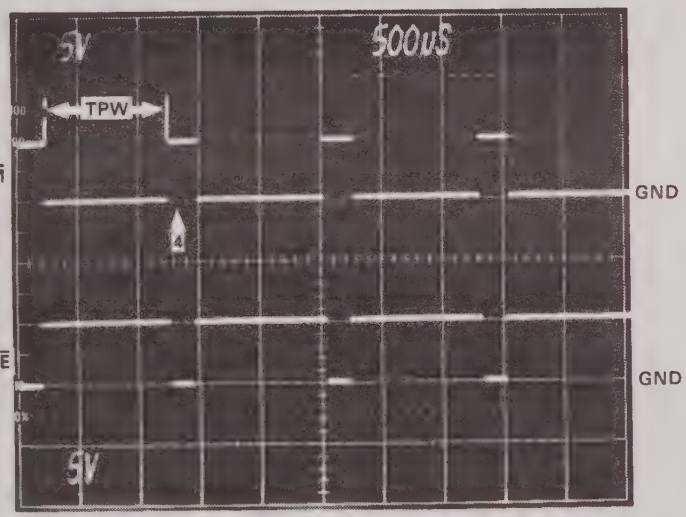
DATA I/O


5V
500uS
2
PGM
GND
BIT TO PROG
GND
5V

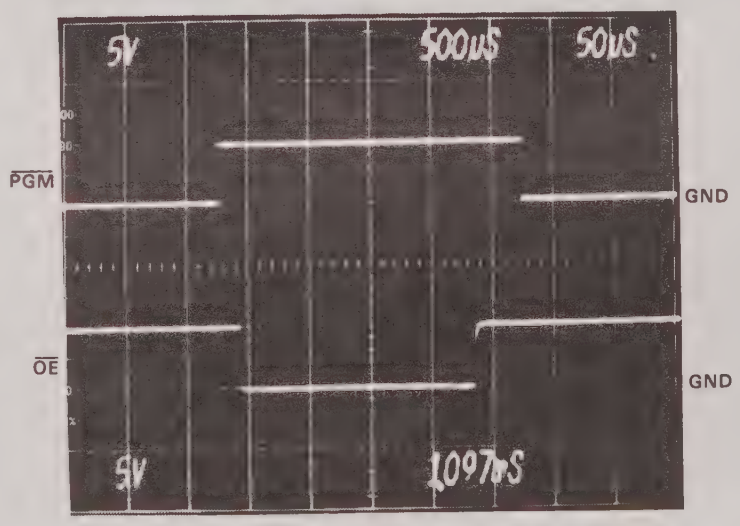
1


5V
500uS
50uS
PGM
GND
BIT TO PROG
GND
5V
1.097mS

2


5V
500uS
TPW
PGM
GND
4
OE
GND
5V

3


5V
500uS
50uS
PGM
GND
OE
GND
5V
1.097mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}	21.0	21.5	22.0	V	Not shown
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	See note 3
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family AF.*
2. *Load RAM with hex 01 for Family BO and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *The overprogram pulse is 2 ms long; see photos 6 and 7.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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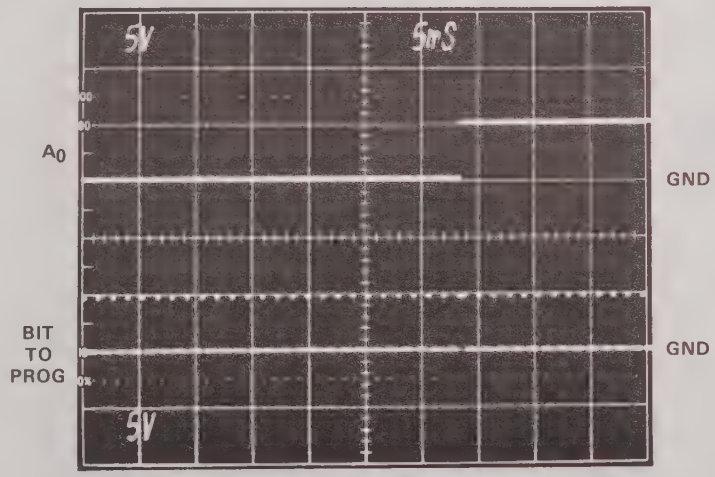
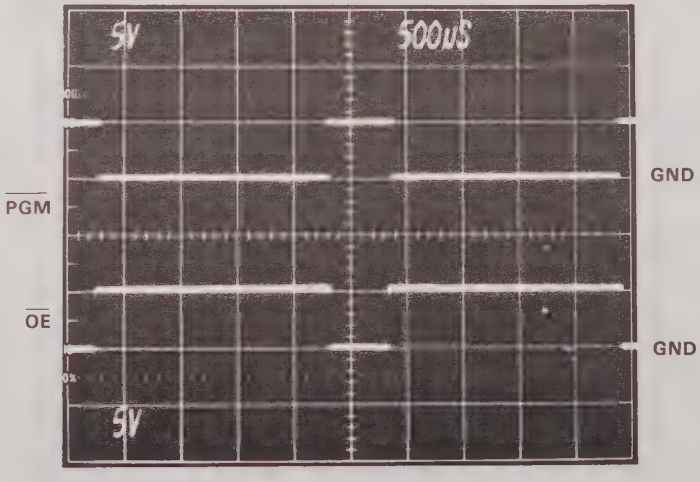
TIMING DIAGRAM

FAMILY CODES AF, BO

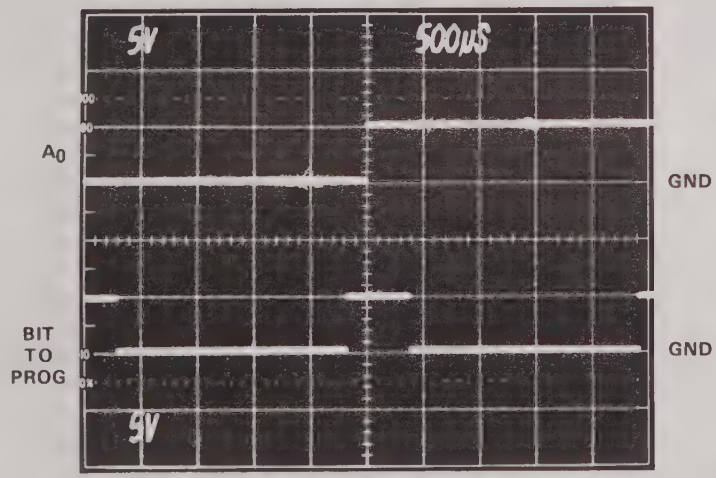
DATA I/O


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
500uS
GND
PGM
OE
GND
5V

6


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

7

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	ECN #5022	CTS	3/84

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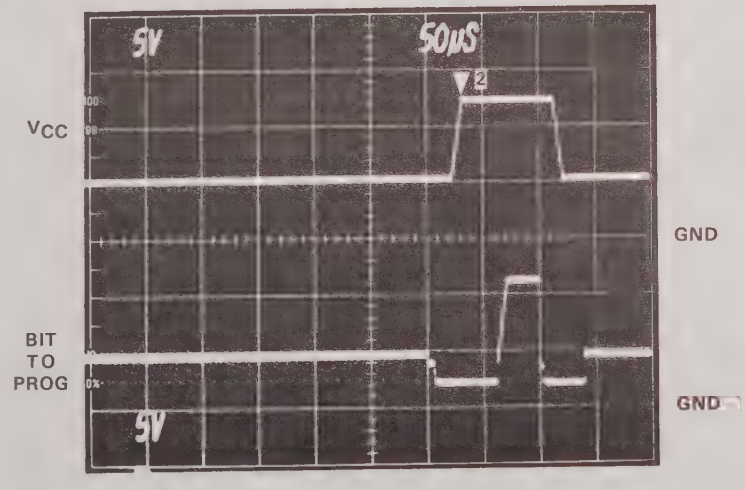
TIMING DIAGRAM

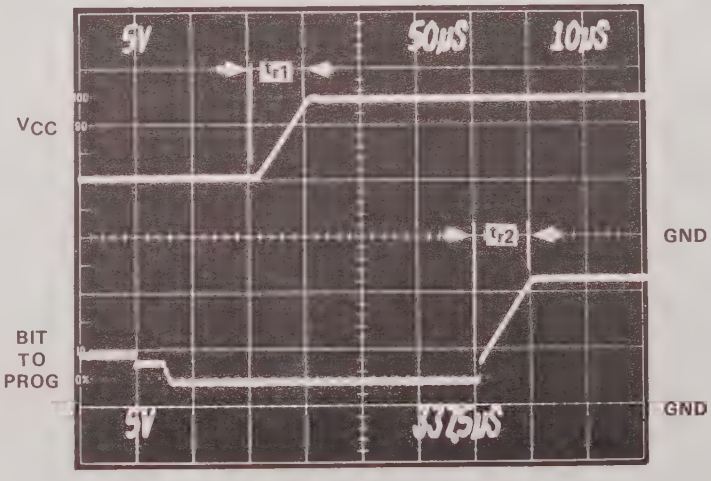
FAMILY CODES AF, BO

DATA I/O

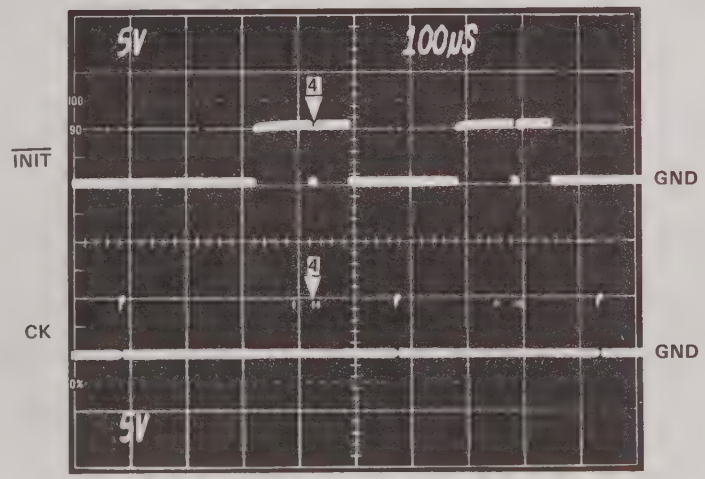
0526/1282


5V
50µS
2
VCC
GND
BIT
TO
PROG
GND
5V

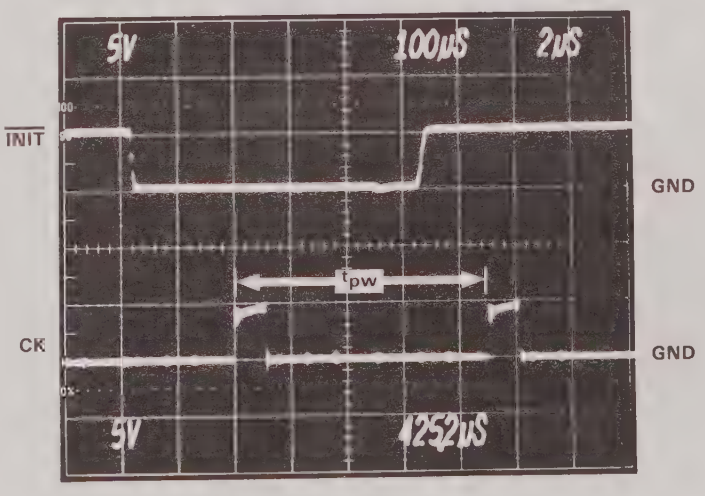
1


5V
50µS
10µS
tr1
VCC
GND
tr2
BIT
TO
PROG
GND
5V
337.5µS

2


5V
100µS
4
INIT
GND
4
CK
GND
5V

3


5V
100µS
2µS
INIT
GND
tpw
CK
GND
5V
1252µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	11.6	11.8	12.0	V	
	V_{OP}	10.5	11.0	11.5	V	
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	9.0	10.0	11.5	us	
	t_{r1}	1.0		20.0	us	See Note 3
	t_{r2}	1.0		15.0	us	
	t_f					N.A.
	Reject		10		PULSES	
	Overprogram		0		PULSES	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	3.4	3.5	3.6	V	701-1998/TP4
	HIGH LOAD	7.7	8.7	9.7	V	701-1998/TP2
	LOW LOAD	7.7	8.7	9.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B1.*
2. *Load RAM with hex 01 for Family B2.*
3. *Load V_{CC} with a 330 Ω, ½-watt resistor.*

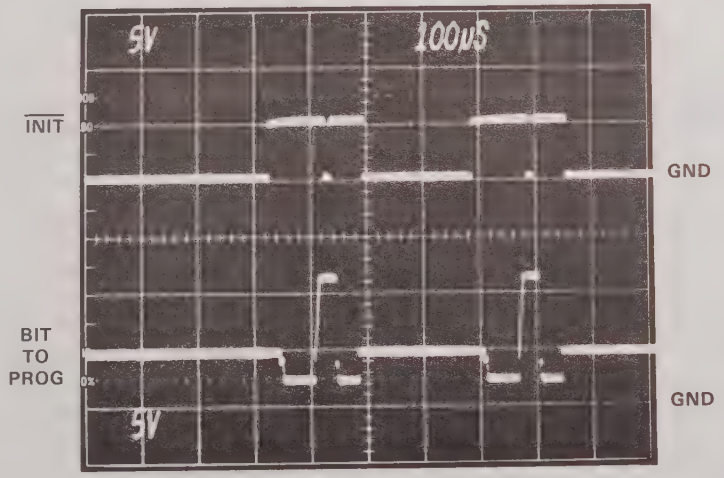
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

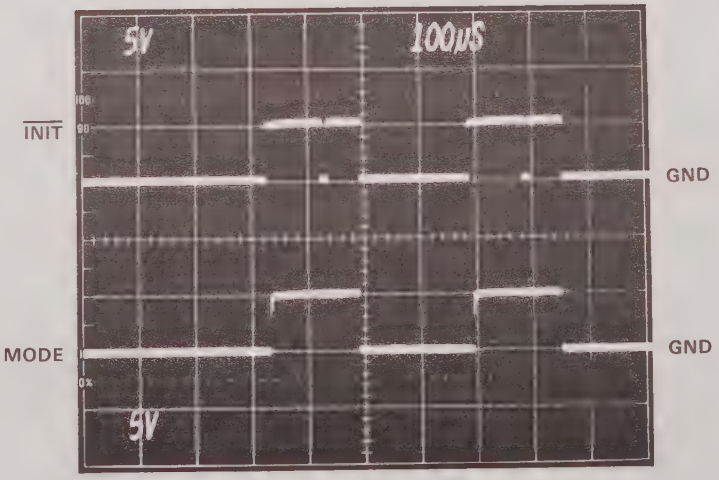
TIMING DIAGRAM

FAMILY CODES B1, B2

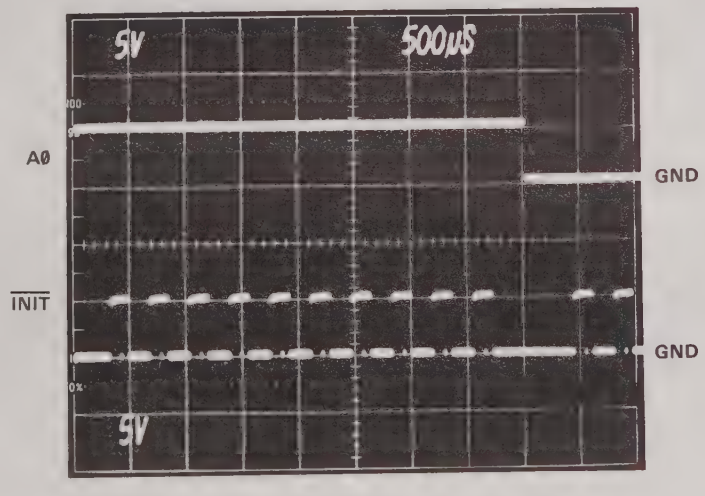
DATA I/O


5V
100µS
INIT
GND
BIT
TO
PROG
GND
5V

5


5V
100µS
INIT
GND
MODE
GND
5V

6


5V
500µS
A0
GND
INIT
GND
5V

7

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	ECN #5022	CTJ	3/84

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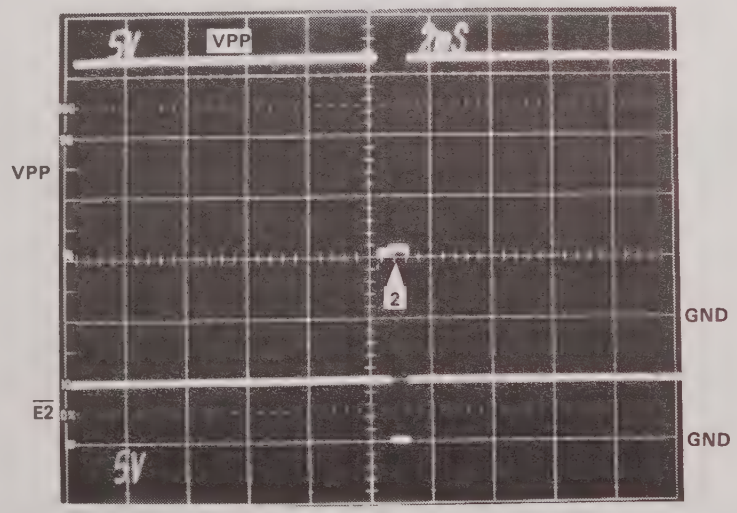
TIMING DIAGRAM

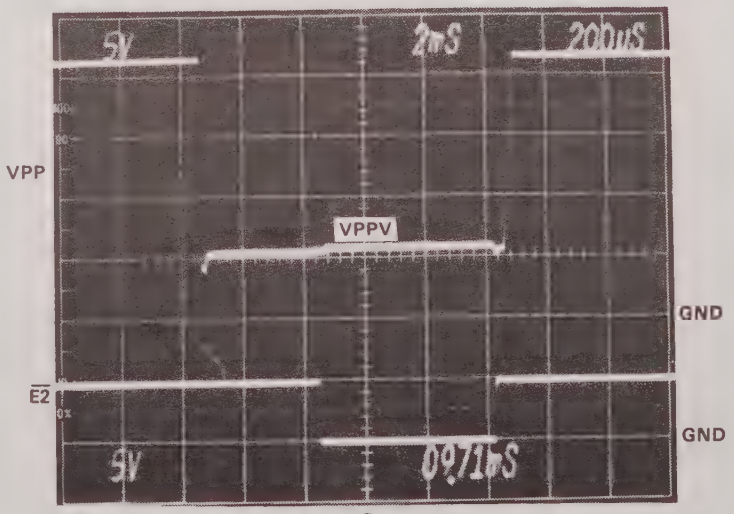
FAMILY CODES B1, B2

DATA I/O

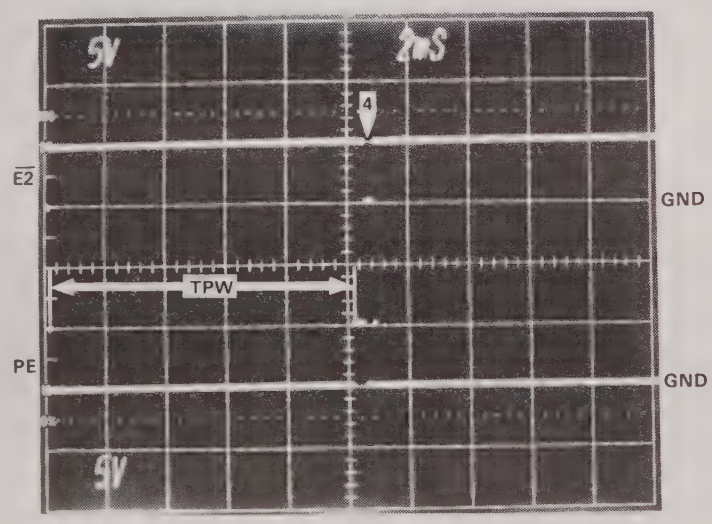
0526/1282


5V
VPP
2mS
VPP
2
GND
E2
GND
5V

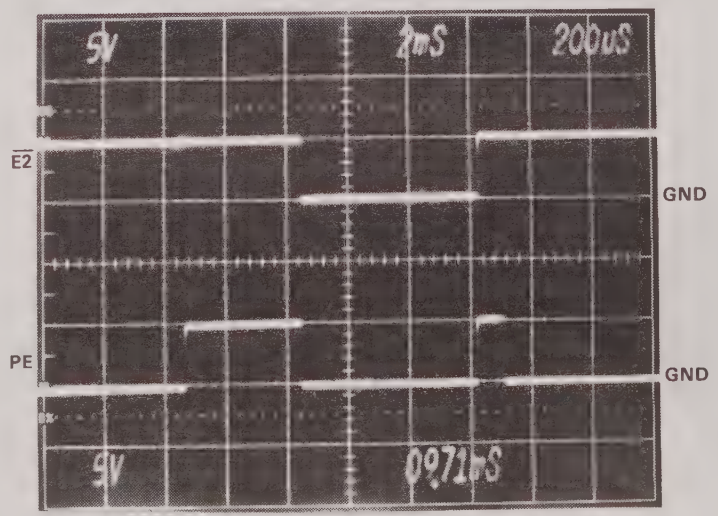
1


5V
2mS
200uS
VPP
VPPV
GND
E2
GND
5V
0971uS

2


5V
2mS
4
E2
GND
TPW
PE
GND
5V

3


5V
2mS
200uS
E2
GND
PE
GND
5V
0971uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					NA
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	VEE	9.0	12.0	15.0	V	
	TPW	9.0		15.0	ms	
	TR					NA
	TF					NA
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B3.*
2. *Load RAM with hex 01 for Family B4 and bit-to-prog waveform becomes bit-no-prog waveform.*
3. *Chip erase waveforms are photos 8 and 9.*
4. *Byte erase waveforms are photos 10 and 11.*

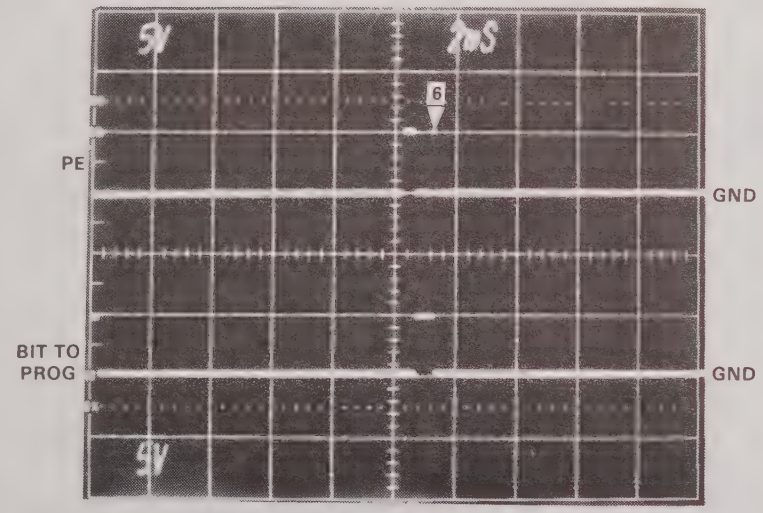
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

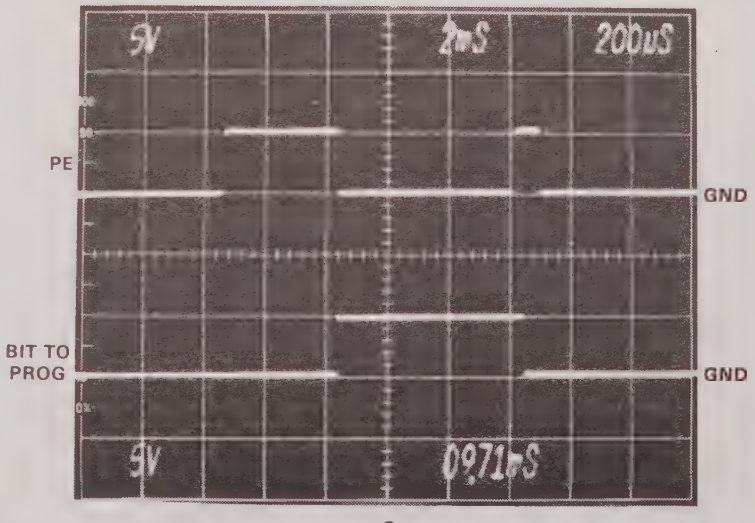
TIMING DIAGRAM

FAMILY CODES B3, B4

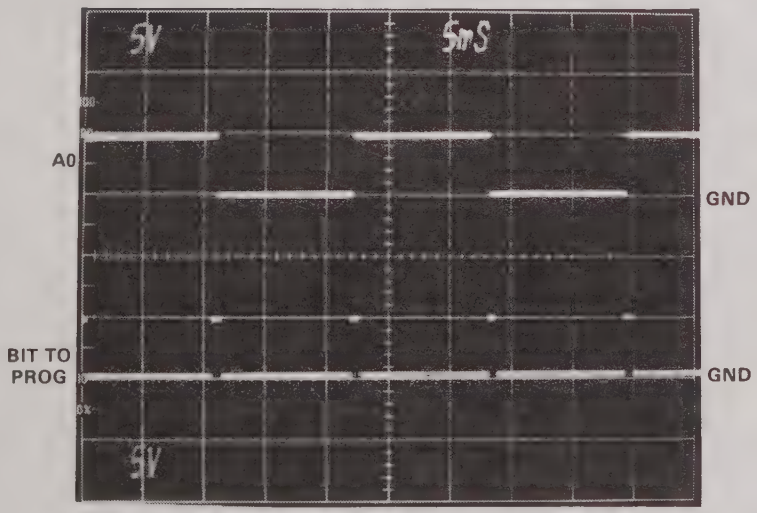
DATA I/O


5V
2mS
6
PE
GND
BIT TO
PROG
GND
5V

5


5V
2mS
200uS
PE
GND
BIT TO
PROG
GND
5V
0.971mS

6


5V
5mS
A0
GND
BIT TO
PROG
GND
5V

7

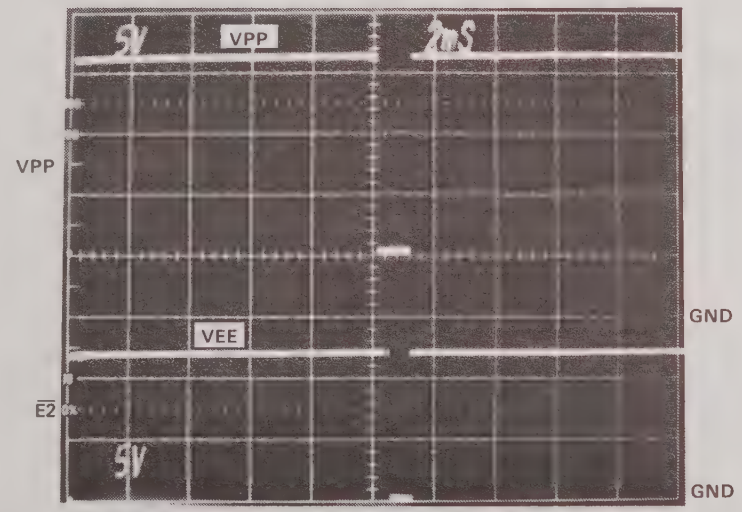
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

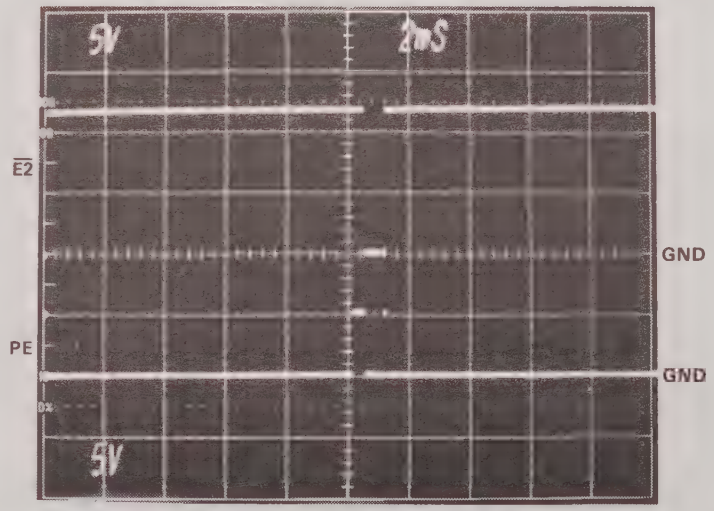
TIMING DIAGRAM

FAMILY CODES B3, B4

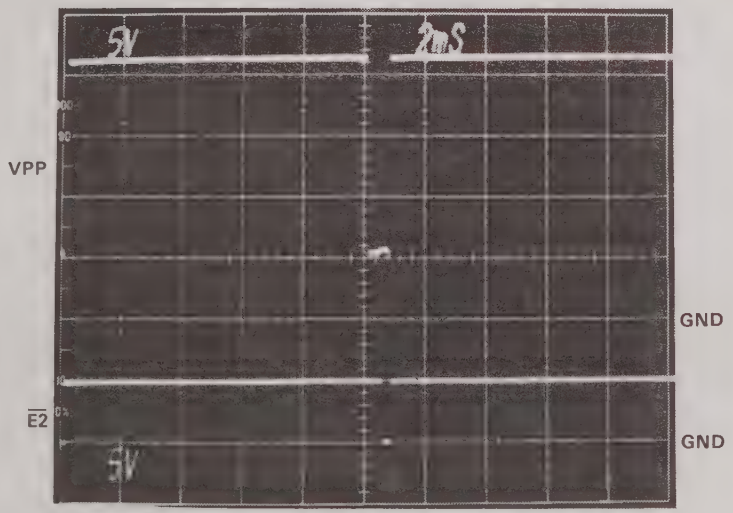
DATA I/O


5V
VPP
2mS
VPP
VEE
GND
E2
5V
GND

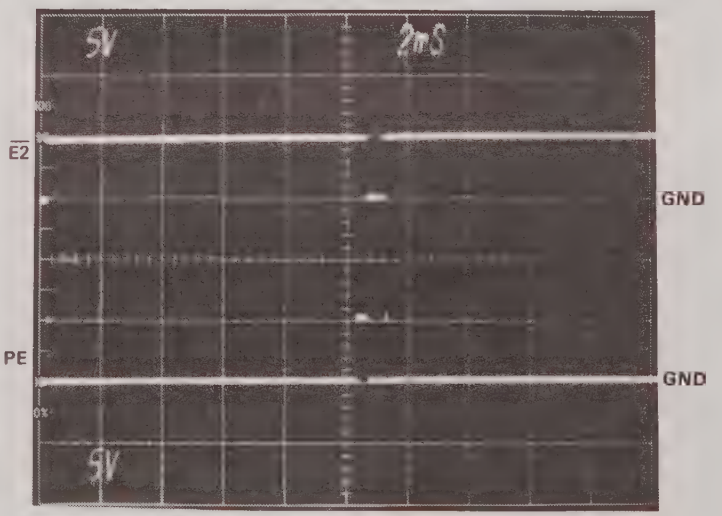
8


5V
2mS
E2
GND
PE
GND
5V

9


5V
2mS
VPP
GND
E2
GND
5V

10


5V
2mS
E2
GND
PE
GND
5V

11

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTB	3/84

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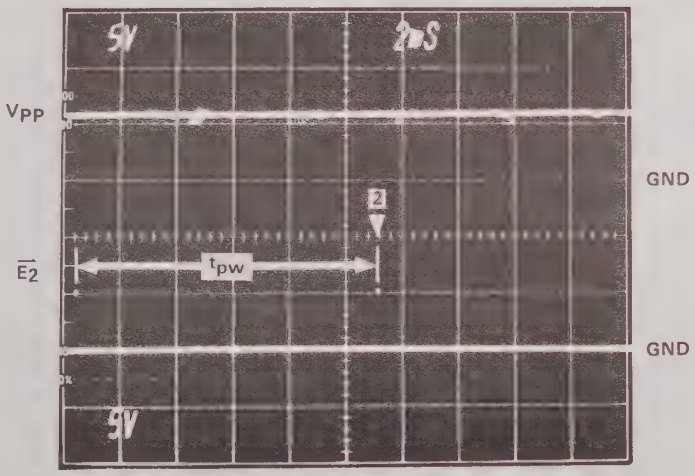
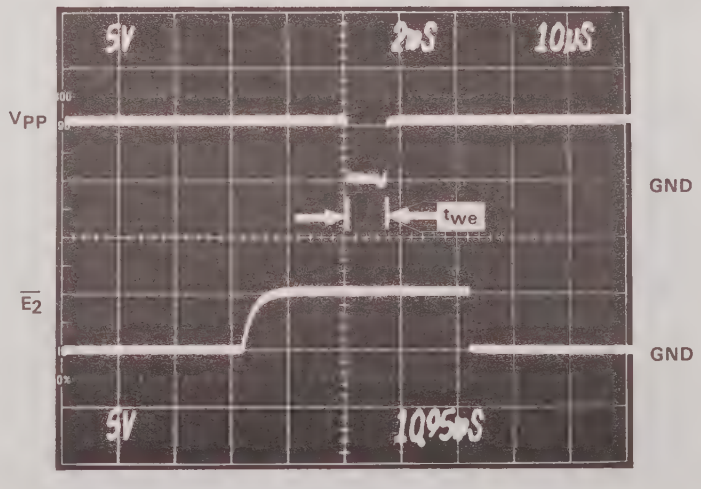
TIMING DIAGRAM

FAMILY CODES B3, B4

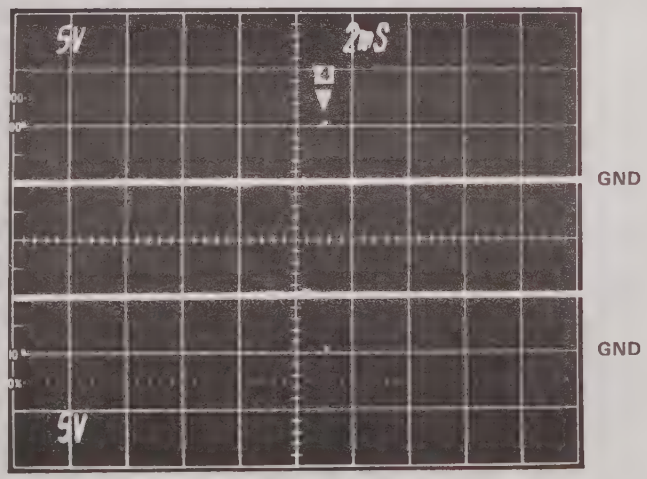
DATA I/O


5V
2mS
VPP
GND
2
$\overline{E_2}$
tpw
GND
5V

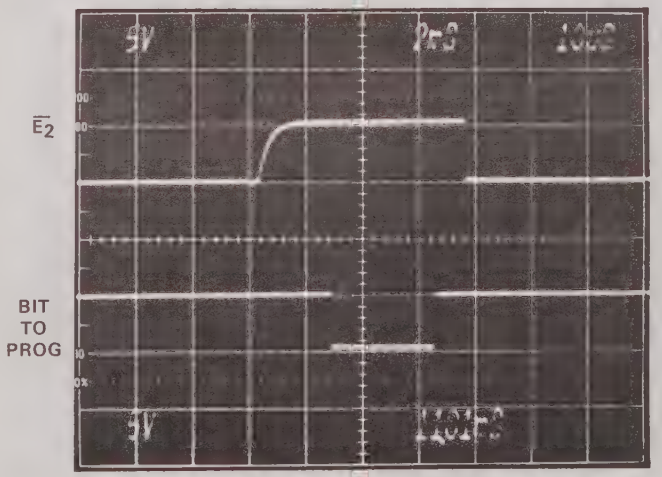
1


5V
2mS
10µS
VPP
GND
twe
$\overline{E_2}$
GND
5V

2


5V
2mS
4
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

3


5V
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EP}	20.5	21.0	21.5	V	
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	150			ns	
	t_{pw}	9	10		ms	
	t_r					N.A.
	t_{ew}	9	10	15	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.1	22.1	23.1	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B7.*
2. *Load RAM with hex 01 for Family B8.*
3. *Photo 6 shows erase pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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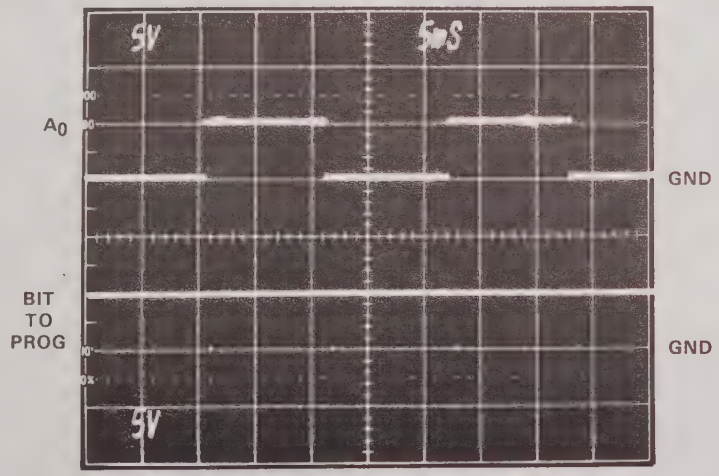
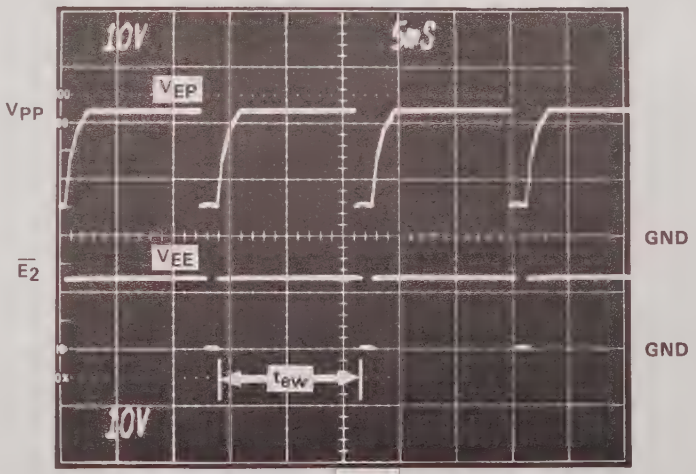
TIMING DIAGRAM

FAMILY CODES B7, B8

DATA I/O


5V
5μS
A0
GND
BIT
TO
PROG
GND
5V

5


10V
5μS
VEP
VPP
GND
VEE
E2
GND
tew
10V

6

B-191
981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTS	3/84

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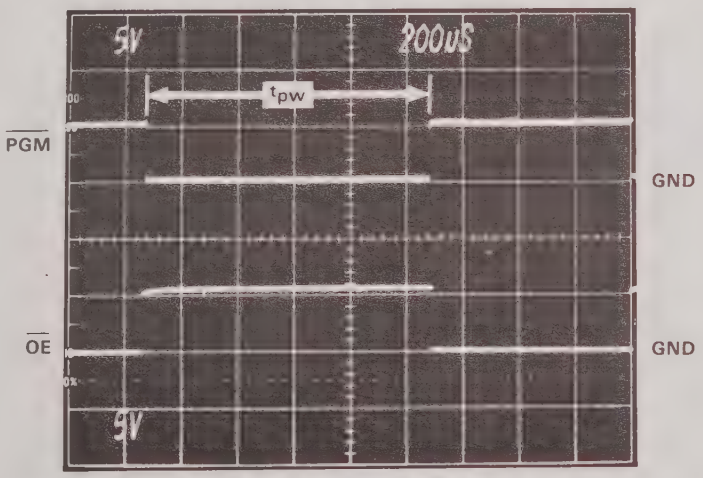
TIMING DIAGRAM

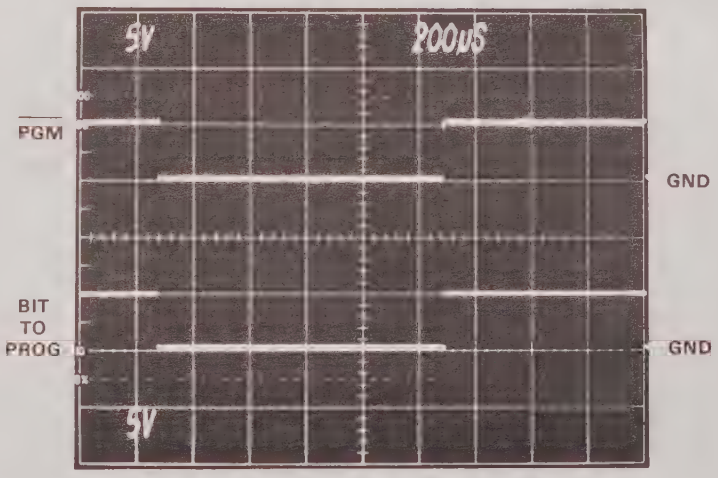
FAMILY CODES B7, B8

DATA I/O

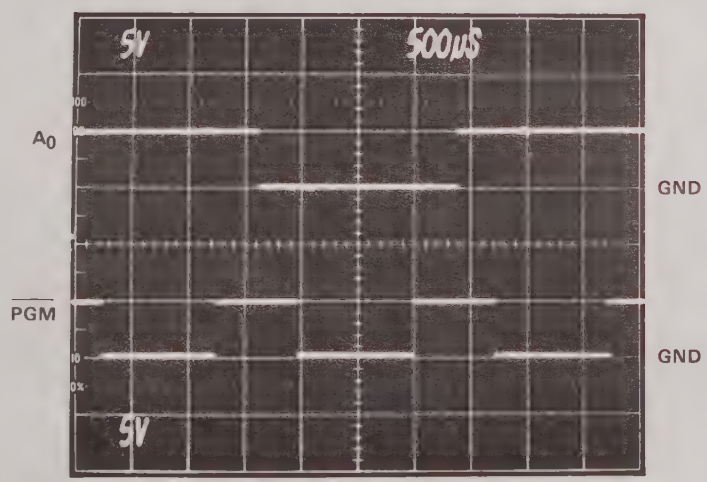
0526/1282


5V
200µS
t_{pw}
PGM
GND
OE
GND
5V

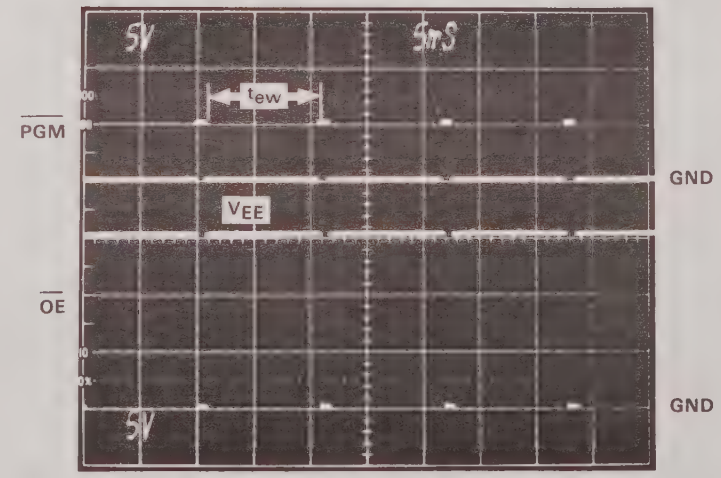
1


5V
200µS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500µS
A_0
GND
PGM
GND
5V

3


5V
5mS
t_{ew}
PGM
GND
V_{EE}
OE
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.0	14.5	15.0	V	
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B9.*
2. *Photo 4 is chip erase.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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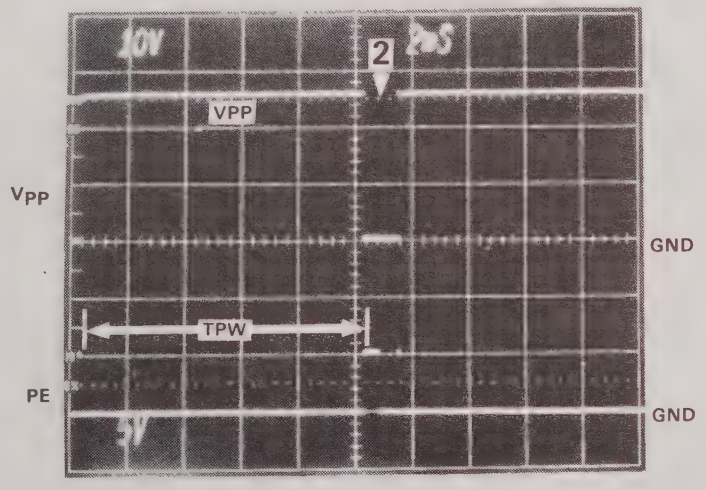
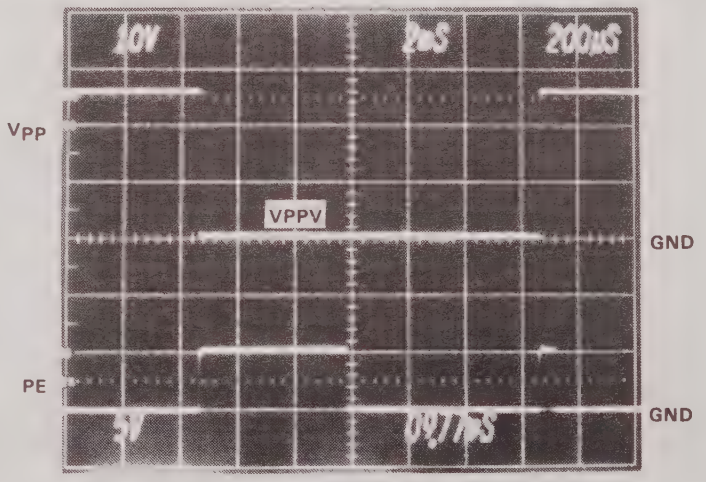
TIMING DIAGRAM

FAMILY CODES B9, BA

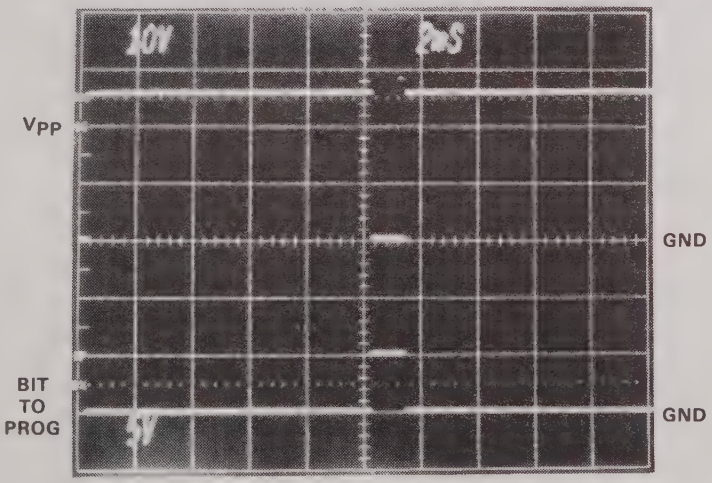
DATA I/O


10V
2mS
2
VPP
VPP
GND
TPW
PE
5V
GND

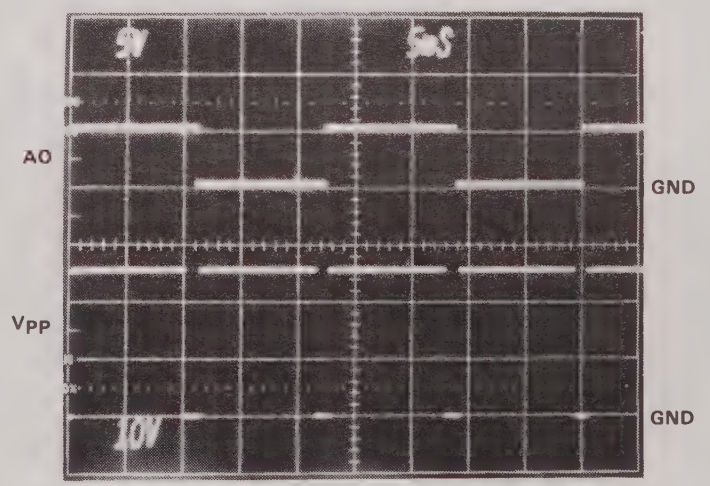
1


10V
2mS
200µS
VPP
VPPV
GND
PE
5V
GND

2


10V
2mS
VPP
GND
BIT
TO
PROG
5V
GND

3


5V
5mS
AO
GND
VPP
10V
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	24.5	25.0	25.5	V	
	V_{PPV}	0.0	0.0	0.5	V	
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family BD.*
2. *Photo 1 is for Pinout 24.*
   Photo 5 is for Pinout 23.
   Photo 6 is for Pinouts 25 and 30.

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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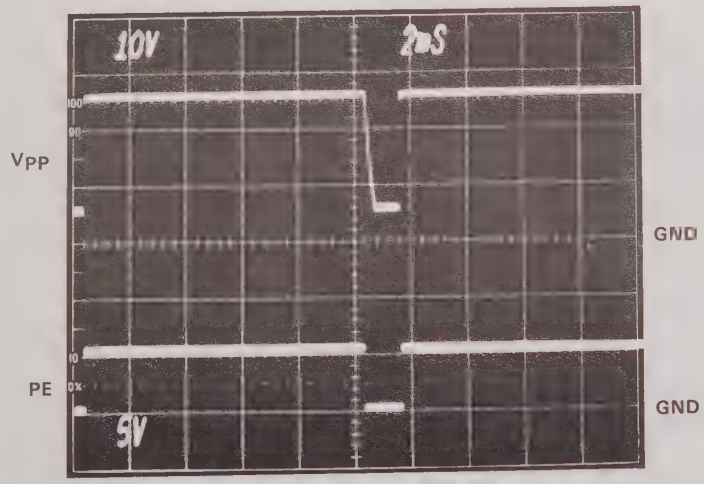
Sheet 1 of 2

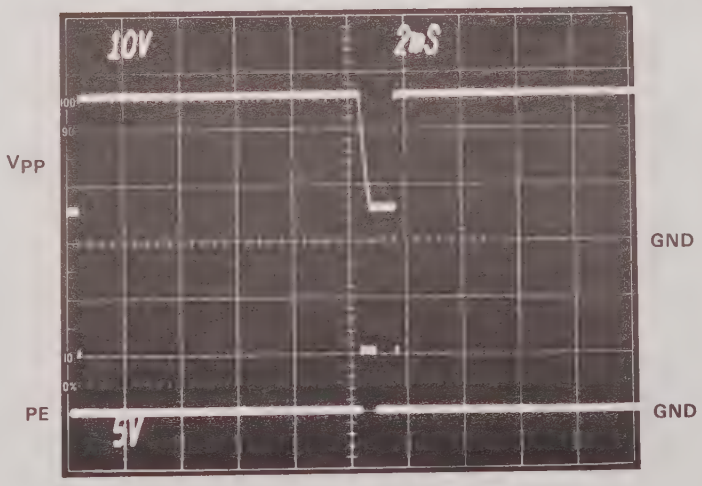
TIMING DIAGRAM

FAMILY CODES BD, BE

DATA I/O



5



6

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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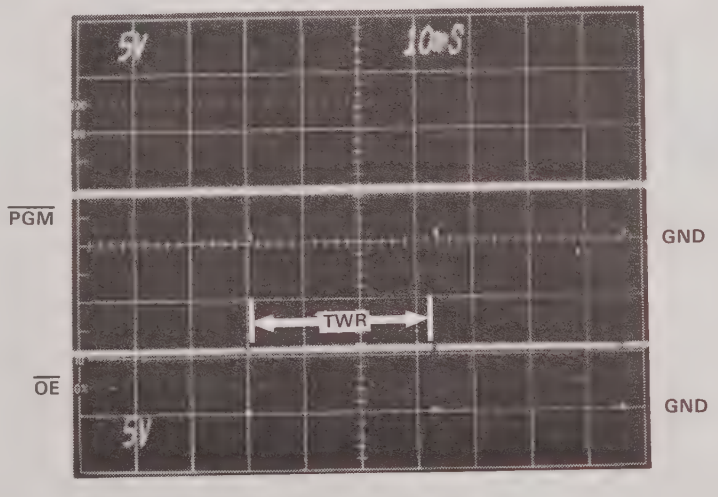
TIMING DIAGRAM

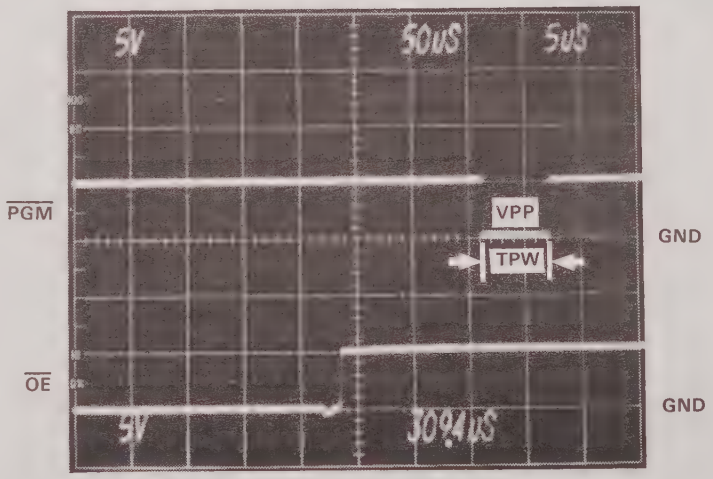
FAMILY CODES BD, BE

DATA I/O

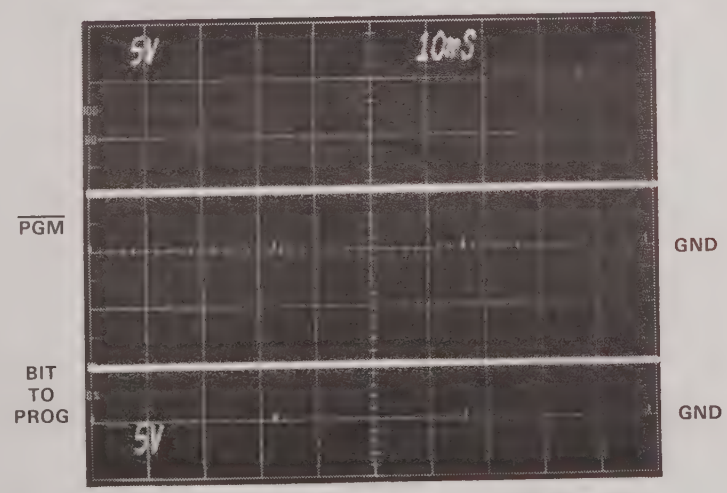
0526 1282


5V
10mS
PGM
GND
TWR
OE
GND
5V

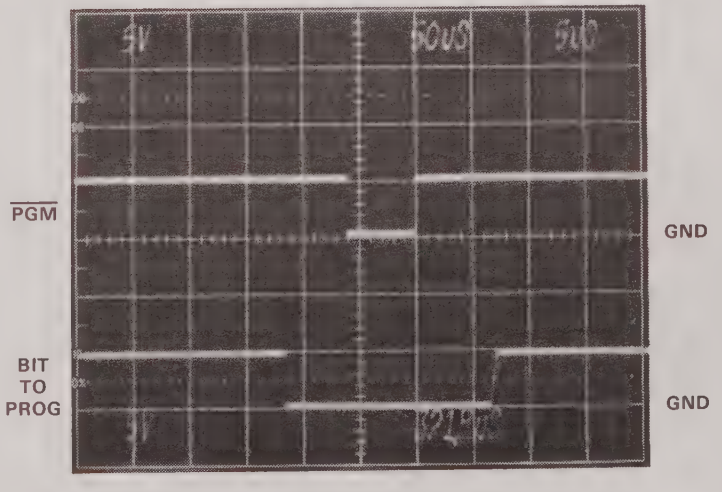
1


5V
50uS
5uS
PGM
VPP
TPW
GND
OE
GND
5V
30%uS

2


5V
10mS
PGM
GND
BIT
TO
PROG
GND
5V

3


5V
50uS
5uS
PGM
GND
BIT
TO
PROG
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	0.0	0.0	0.8	V	
	V_{PPV}					N.A.
	t_{pw}	100			ns	
	t_r					N.A.
	t_{wr}	30			ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family BF.*
2. *Load pin 1 with a 330 Ω, ½-watt resistor to observe TWR in photos 1, 3 and 5.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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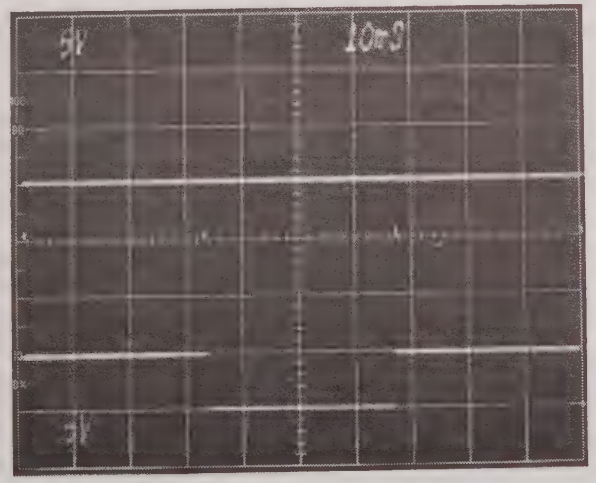
TIMING DIAGRAM

FAMILY CODES BF, CO

DATA I/O



5

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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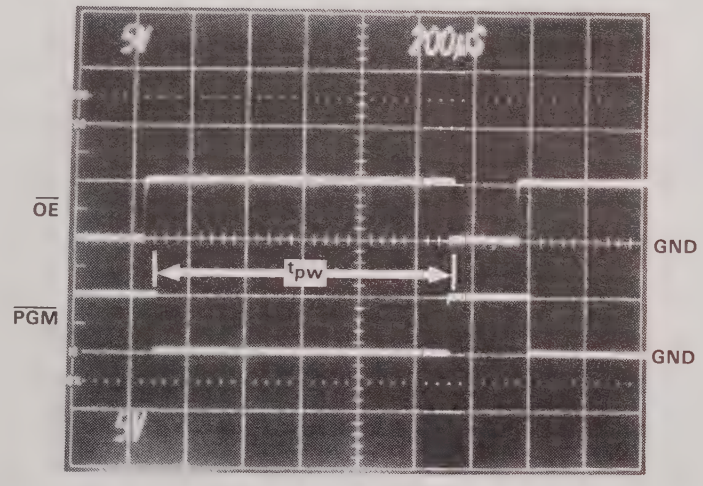
TIMING DIAGRAM

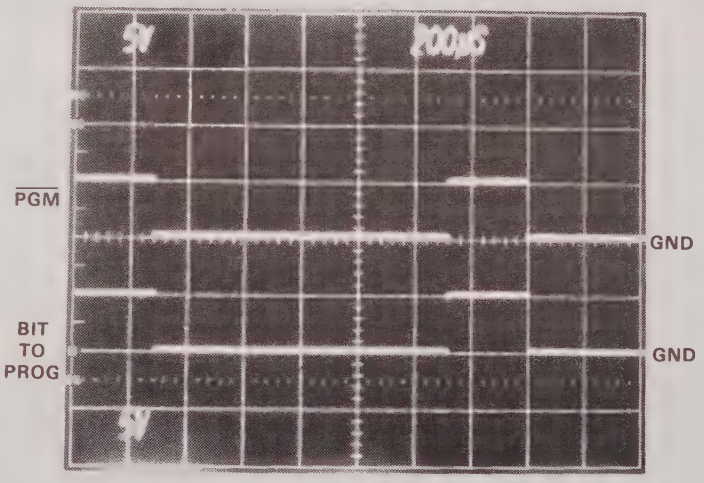
FAMILY CODES BF, CO

DATA I/O

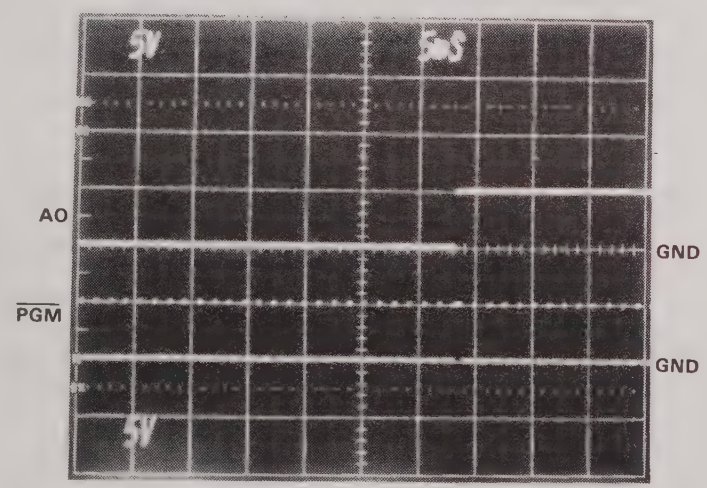
0526/1282


5V
200μS
OE
GND
tpw
PGM
GND
5V

1


5V
200μS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
5mS
AO
GND
PGM
GND
5V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	Not Shown
	V_{PPV}					
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSE	
	Overprogram		1		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. Load RAM with hex FE for Family C1.

REVISIONS

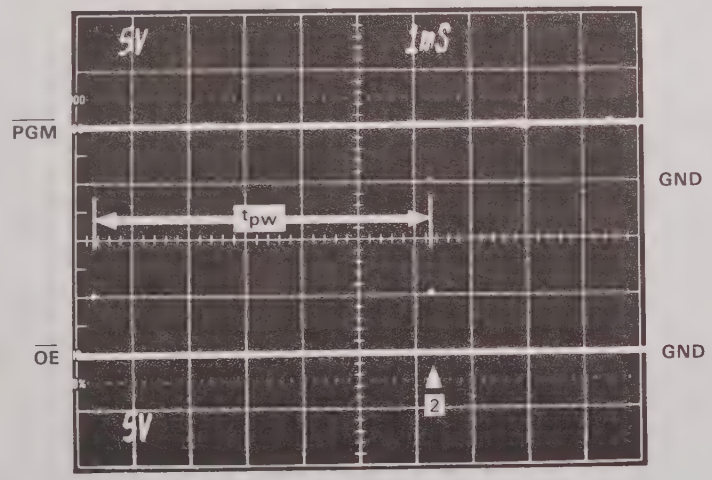
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

Sheet 1 of 1

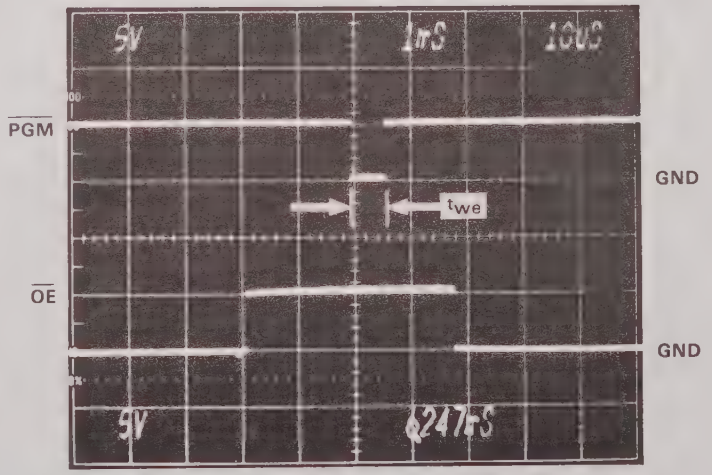
TIMING DIAGRAM

FAMILY CODES C1, C2

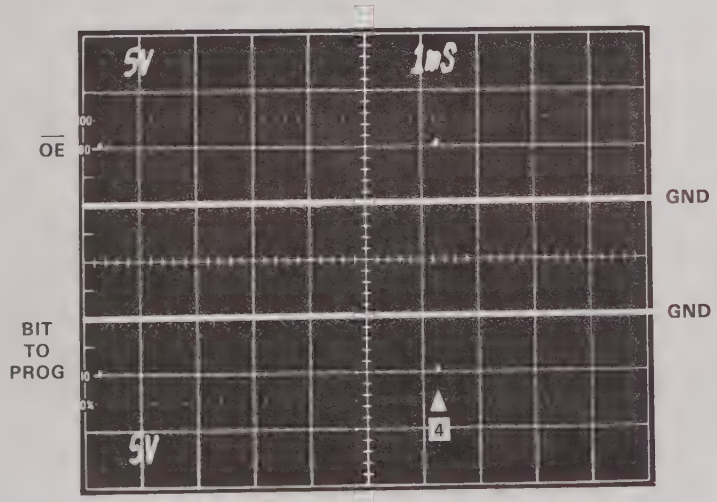
DATA I/O


5V
1mS
PGM
GND
t_{pw}
OE
GND
2
5V

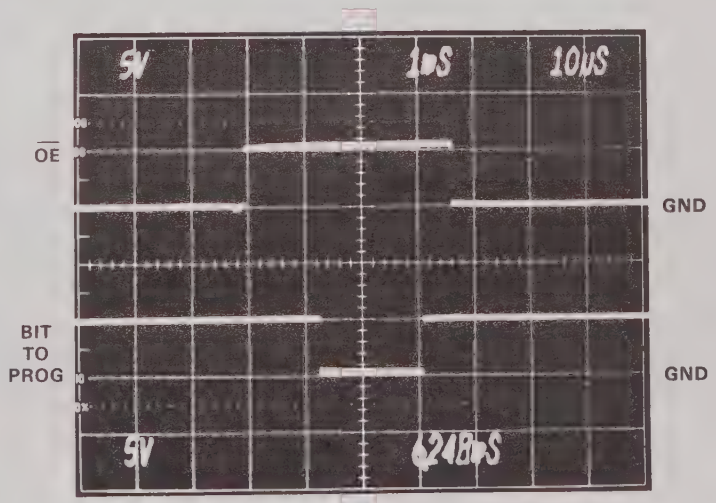
1


5V
1mS
10uS
PGM
GND
t_{we}
OE
GND
5V
6.247mS

2


5V
1mS
OE
GND
GND
BIT
TO
PROG
4
5V

3


5V
1mS
10uS
OE
GND
BIT
TO
PROG
GND
5V
6.248mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	14.5	15.0	15.5	V	
	t_{we}	150			ns	
	t_{pw}	0.1	5		ms	
	t_r					N.A.
	t_{ew}	150			ns	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.3	0.4	0.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.1	22.1	23.1	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family C3.*
2. *Load RAM with hex 01 for Family C4.*
3. *Photos 6 and 7 show erase pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
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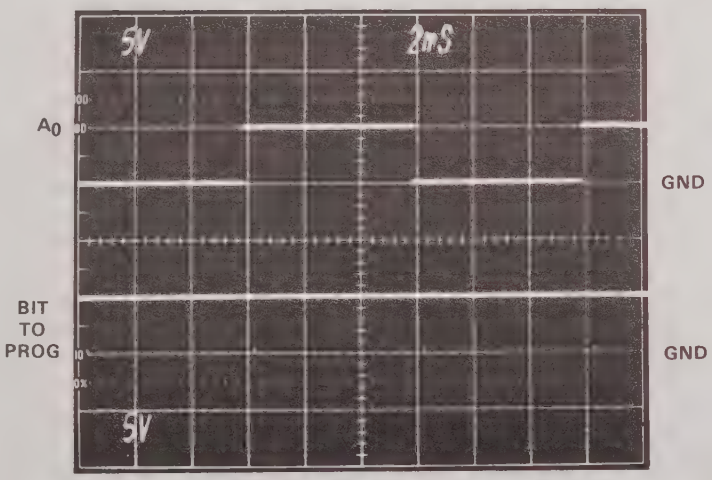
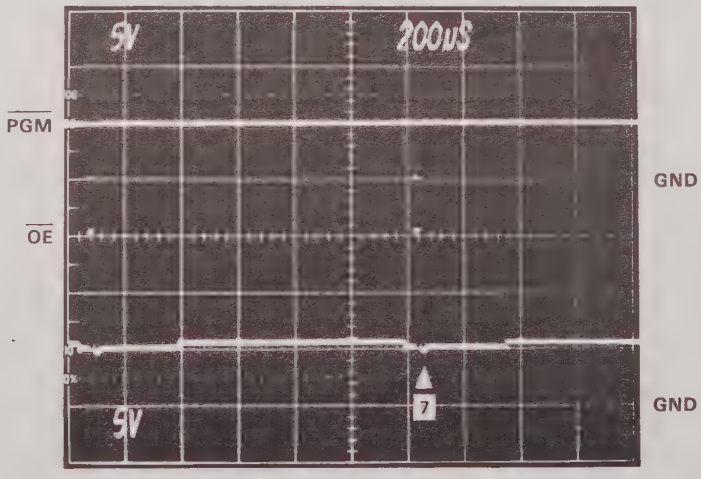
TIMING DIAGRAM

FAMILY CODES C3, C4

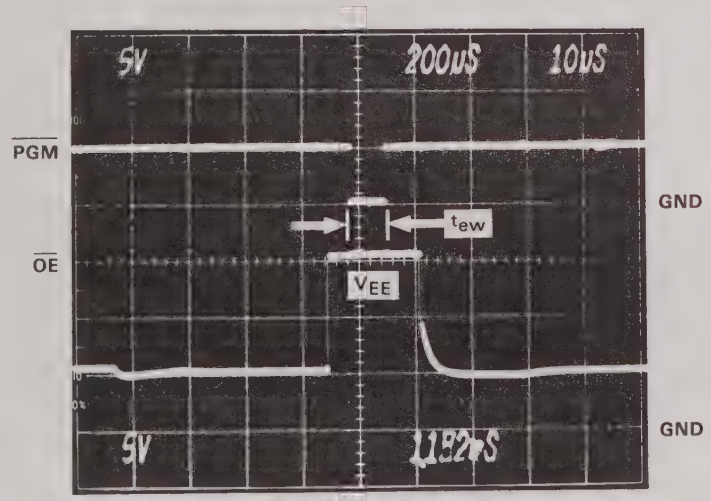
DATA I/O


5V
2mS
A_0
GND
BIT
TO
PROG
GND
5V

5


5V
200uS
PGM
GND
OE
7
GND
5V

6


5V
200uS
10uS
PGM
GND
t_{ew}
OE
V_{EE}
GND
5V
1.152mS

7

REVISIONS

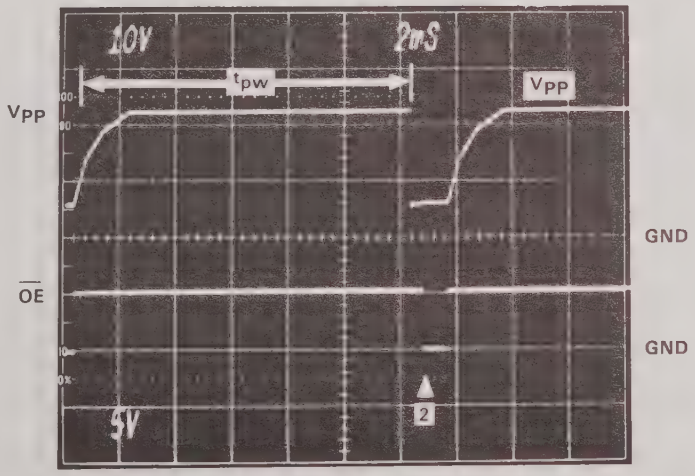
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

Sheet 2 of 2

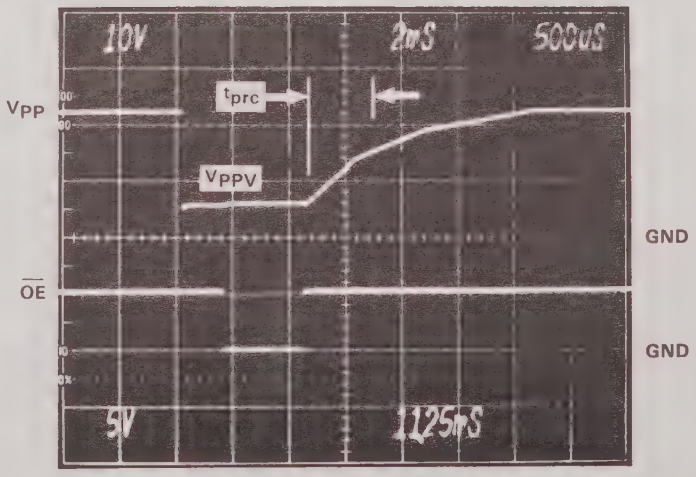
TIMING DIAGRAM

FAMILY CODES C3, C4

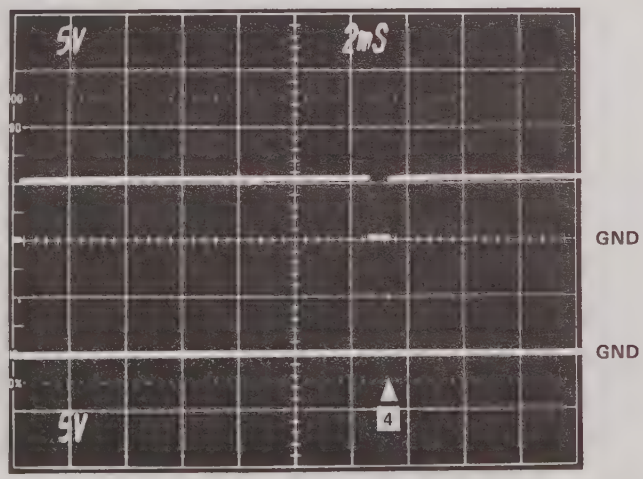
DATA I/O


10V
2mS
tpw
VPP
VPP
GND
OE
GND
5V
2

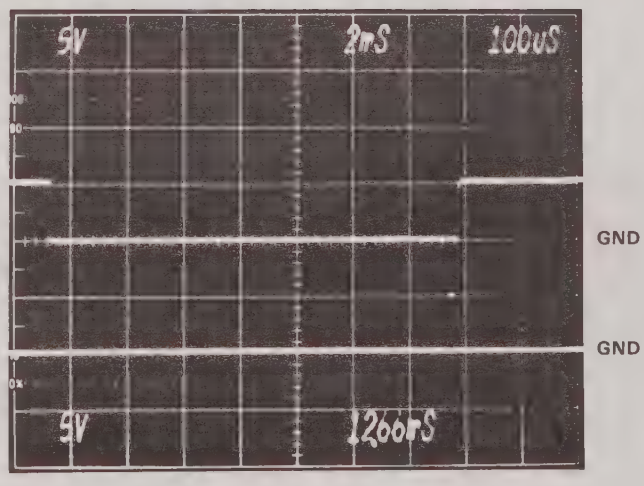
1


10V
2mS
500uS
VPP
tprc
VPPV
GND
OE
GND
5V
1125mS

2


5V
2mS
OE
GND
CE
GND
5V
4

3


5V
2mS
100uS
OE
GND
CE
GND
5V
1266mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	20.0	21.0	22.0	V	
	V_{PPV}	4.0	5.0	6.0	V	
	t_{prc}	450	600	750	μs	See note 3
	t_{pw}	9.0		15.0	ms	
	t_r					N.A.
	t_f			100	μs	
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family C7.*
2. *Load RAM with hex 01 for Family C8.*
3. *TPRC is measured from 6V to 15.5V.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	C7Z	2/84

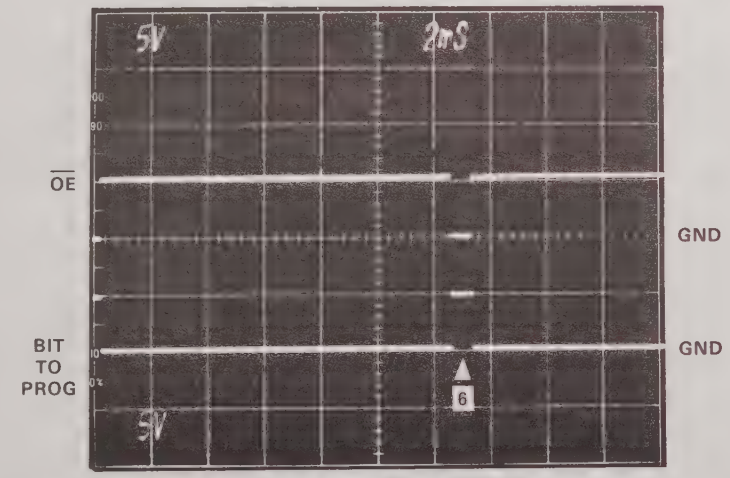
Sheet 1 of 2

TIMING DIAGRAM

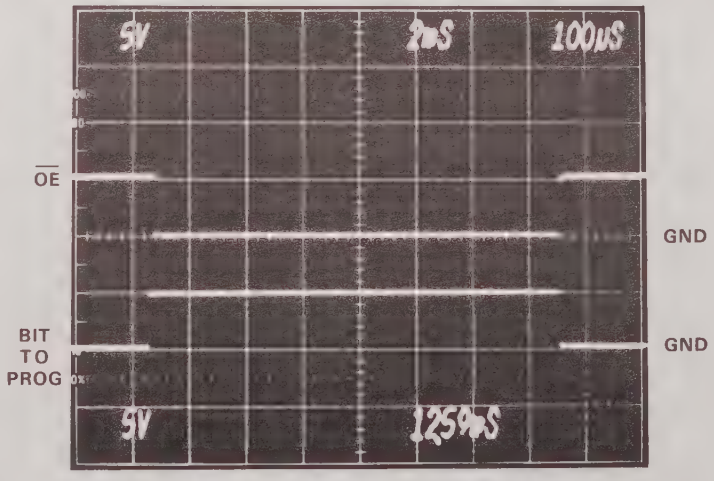
FAMILY CODES C7, C8

DATA I/O

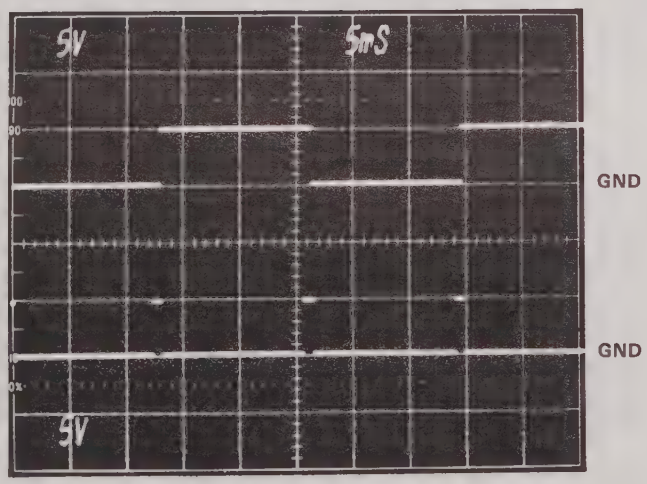
0526/1282


5V
2mS
OE
GND
BIT
TO
PROG
GND
6
5V

5


5V
2mS
100uS
OE
GND
BIT
TO
PROG
GND
5V
1259mS

6


5V
5mS
A0
GND
BIT
TO
PROG
GND
5V

7

B-211
981-0003

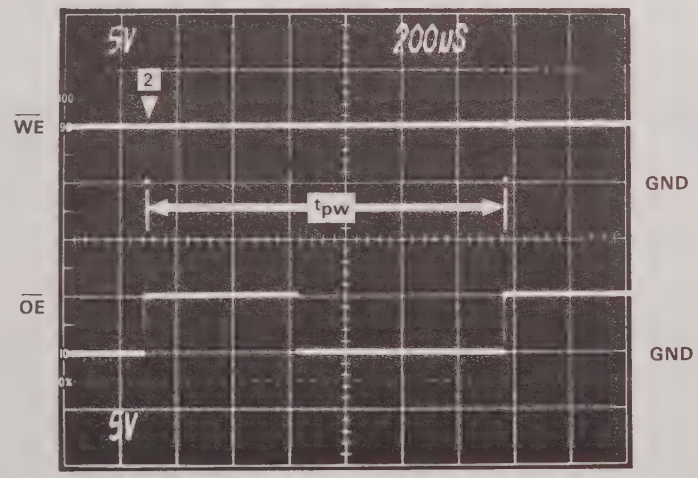
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	C78	3/84

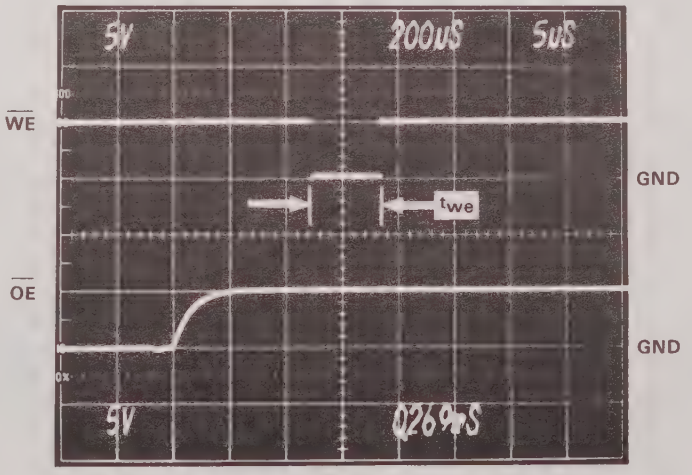
TIMING DIAGRAM

FAMILY CODES C7, C8

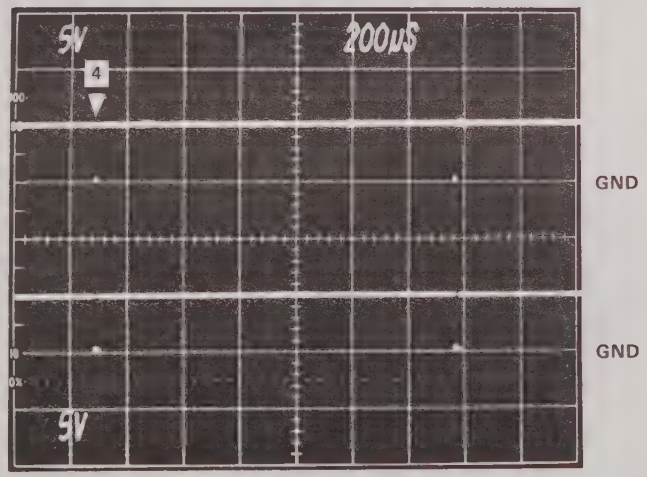
DATA I/O


5V
200uS
2
WE
tpw
GND
OE
GND
5V

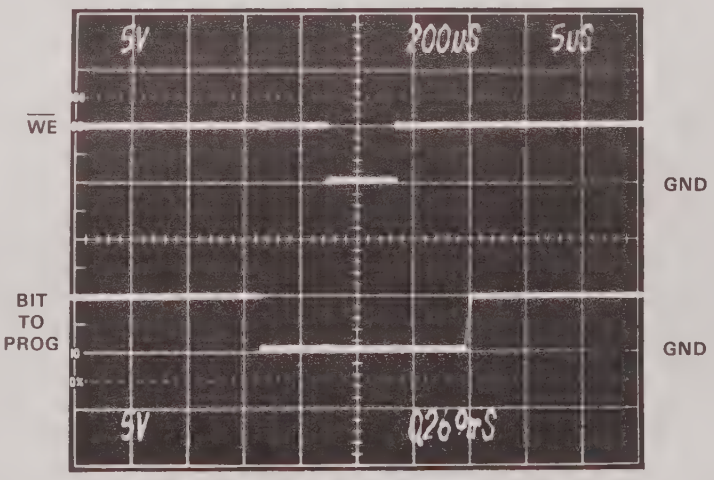
1


5V
200uS
5uS
WE
GND
twe
OE
GND
5V

2


5V
200uS
4
WE
GND
BIT
TO
PROG
GND
5V

3


5V
200uS
5uS
WE
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{we}	70			ns	
	t_{pw}	1.0		25	ms	See note 3
	t_r					N.A.
	t_{ew}	10		12	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family C9.*
2. *Load RAM with hex 01 for Family CA.*
3. *Photo 1 shows min. TPW; photo 6 shows max. TPW (load pin 1 of socket with 100Ω, ¼W resistor to observe waveform photo 6).*
4. *Photo 7 shows erase waveform.*

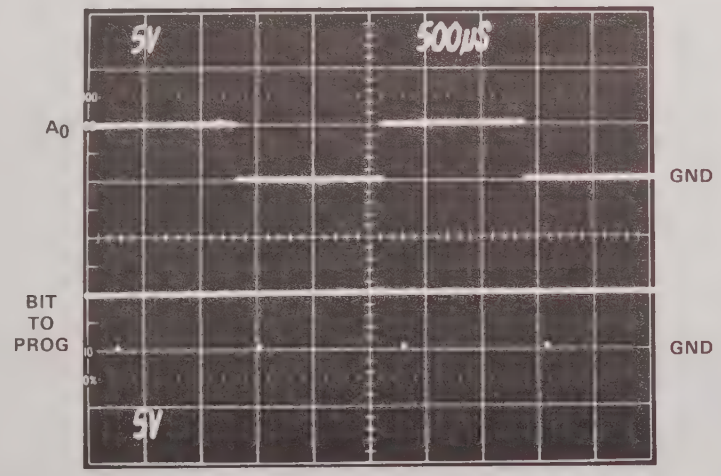
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTS	3/84

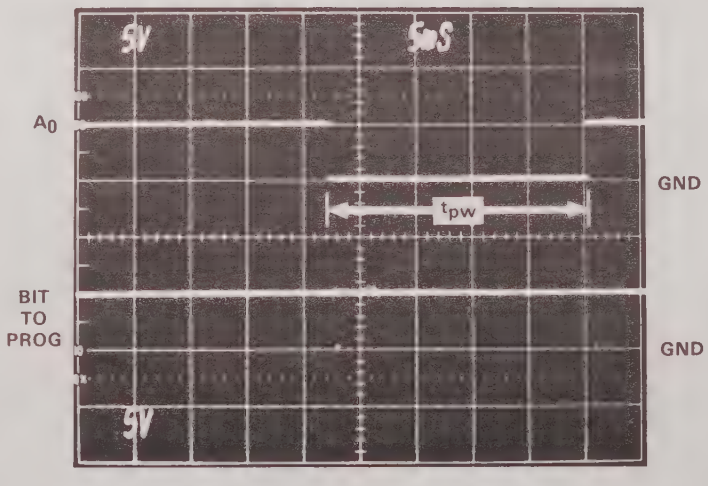
TIMING DIAGRAM

FAMILY CODES C9, CA

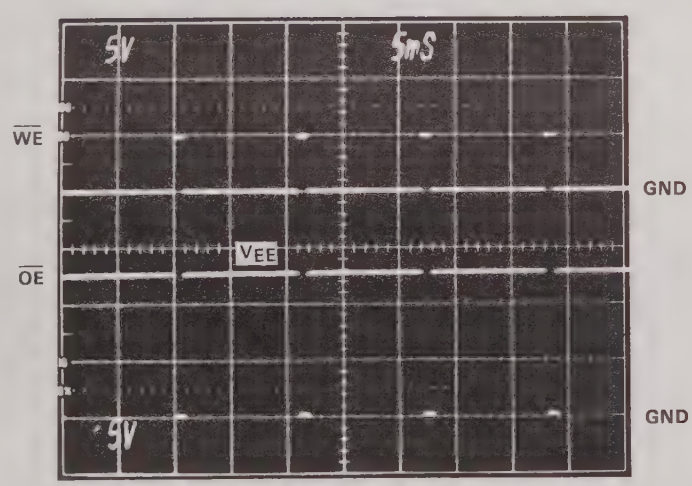
DATA I/O


5V
500µS
A0
GND
BIT
TO
PROG
GND
5V

5


5V
5mS
A0
GND
tpw
BIT
TO
PROG
GND
5V

6


5V
5mS
WE
GND
VEE
OE
GND
5V

7

B-215
981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

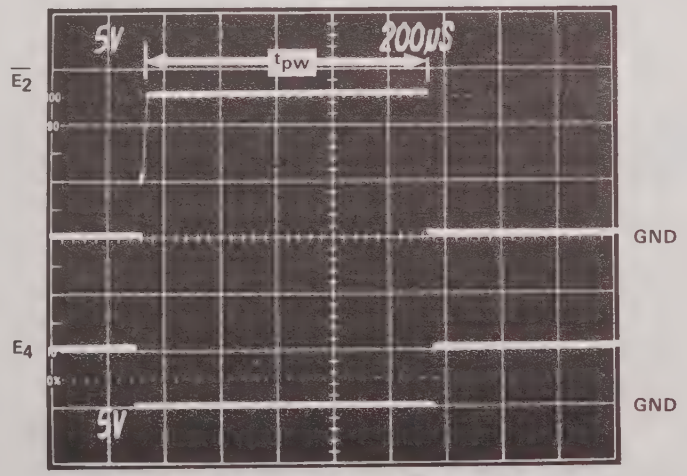
Sheet 2 of 2

TIMING DIAGRAM

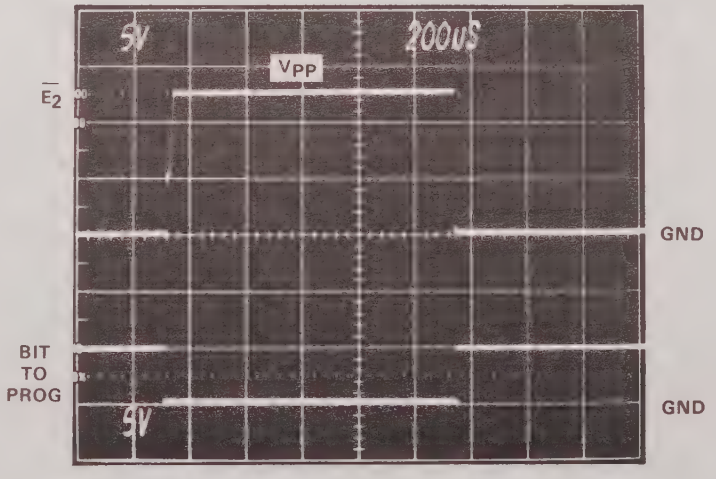
FAMILY CODES C9, CA

DATA I/O

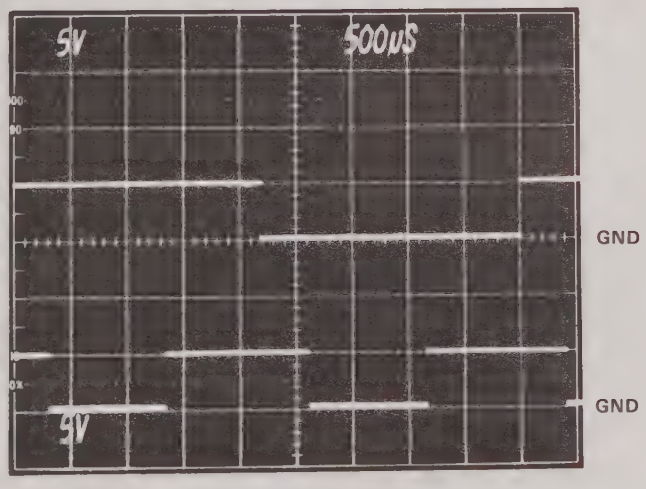
0526/1282


5V
200µS
t_{pw}
$\overline{E_2}$
GND
E_4
GND
5V

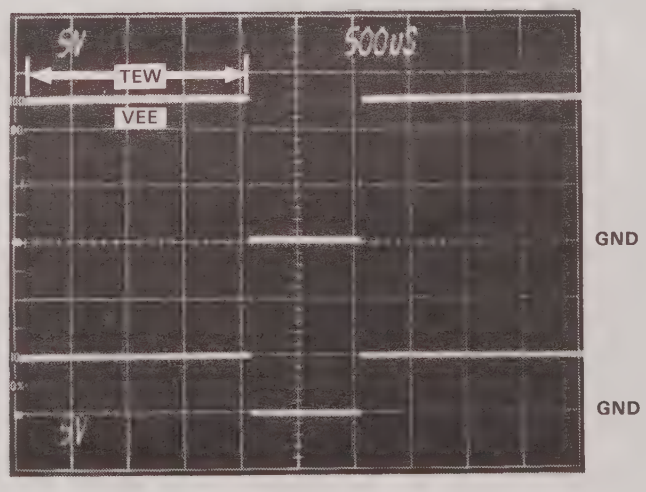
1


5V
200µS
V_{PP}
$\overline{E_2}$
GND
BIT
TO
PROG
GND
5V

2


5V
500µS
A_0
GND
BIT
TO
PROG
GND
5V

3


5V
500µS
TEW
$\overline{E_2}$
VEE
GND
E_4
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	11.5	12.0	12.5	V	
	V_{PPV}					N.A.
	V_{EE}	11.5	12.0	12.5	V	
	t_{pw}	1.0			ms	
	t_r					N.A.
	t_{ew}	2.0			ms	
	t_f					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.4	4.5	4.6	V	
	V_{REF}	0.7	0.8	0.9	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.5	22.5	23.5	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.4	5.5	5.6	V	
	V_{REF}	1.9	2.0	2.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.2	6.7	7.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family CD.*
2. *Load RAM with hex 01 for Family CE.*
3. *Photo 4 shows erase pulse.*

REVISIONS

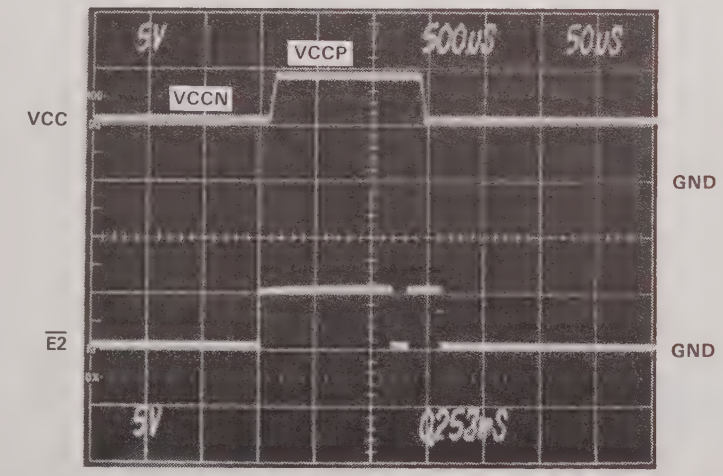
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

Sheet 1 of 1

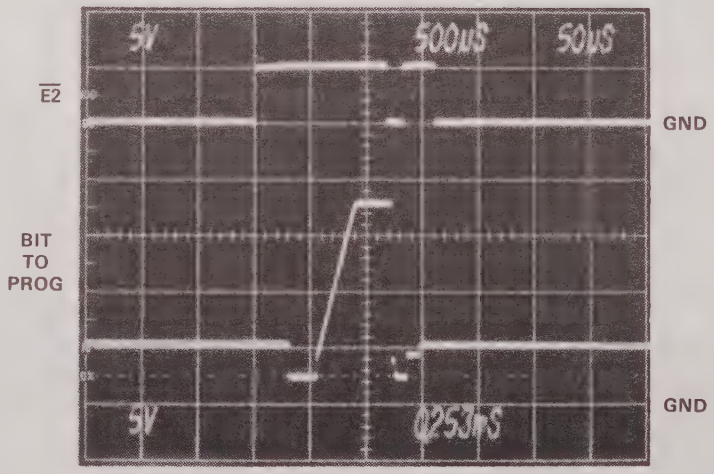
TIMING DIAGRAM

FAMILY CODES CD, CE

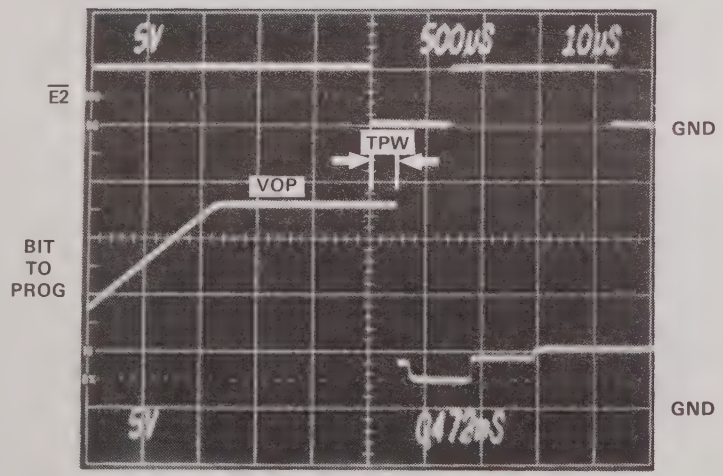
DATA I/O


5V
500uS
50uS
VCCP
VCCN
VCC
GND
E2
GND
5V
@253mS

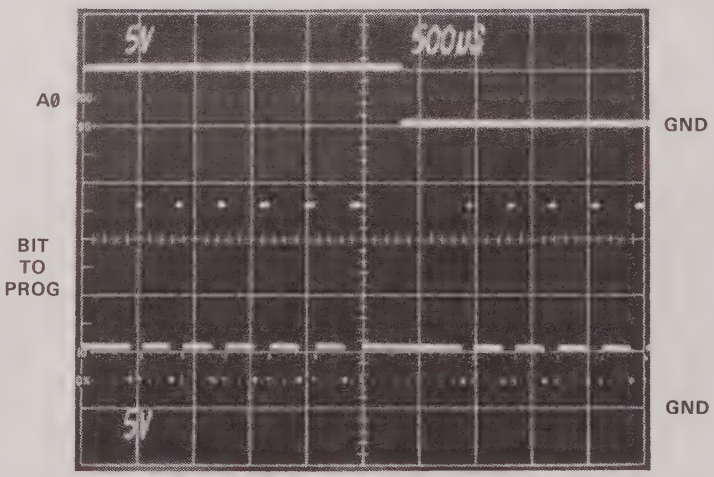
1


5V
500uS
50uS
E2
GND
BIT
TO
PROG
GND
5V
@253mS

2


5V
500uS
10uS
E2
GND
TPW
VOP
BIT
TO
PROG
GND
5V
@472mS

3


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	8.4	8.8	9.2	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	17.0	17.5	18.0	V	
	TPWB	4.7	5.0	5.3	μ	See Note 4
	TPWE	29.5	30.0	30.5	μ	See Note 4
	Reject		6			Pulses
	Overprogram		1			Pulse
	TOP	19.5	20.0	20.5	μ	See Note 5
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.7	0.8	0.9	V	701-1998/TP4
	High Load	23.9	24.9	25.9	V	701-1998/TP2
	Low Load	23.9	24.9	25.9	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	6.2	7.2	8.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family CF.*
2. *Load RAM with hex 01 for Family D0.*
3. *Load VCC with a 100Ω, 2-watt resistor.*
4. *TPW increases from 5 μs to 30 μs in 5 μs increments.*
5. The overprogram TPW is 20 μs. This is not shown.

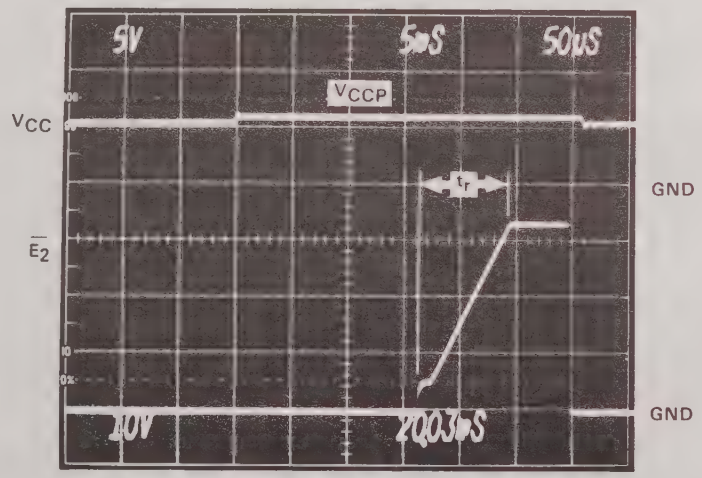
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

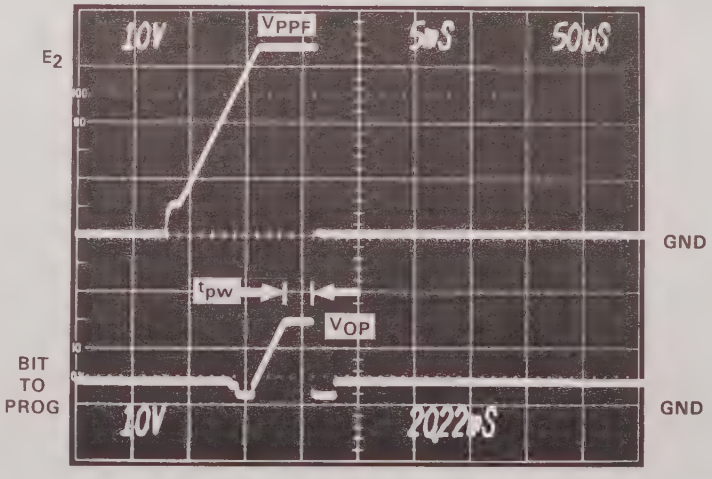
TIMING DIAGRAM

FAMILY CODES CF, D0

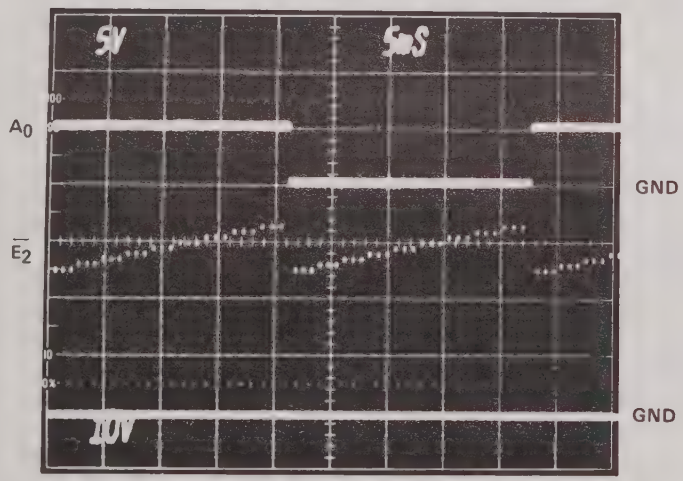
DATA I/O


5V
5mS
50uS
VCCP
VCC
tr
GND
E2
GND
10V
2003mS

1


10V
VPPF
5mS
50uS
E2
GND
tpw
VOP
BIT
TO
PROG
GND
10V
2022mS

2


5V
5mS
A0
GND
E2
GND
10V

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.25	5.5	5.75	V	
	V_{OP}	14.5	15.0	15.5	V	
	V_{PPS}	24.0	25.0	26.0	V	See note 3
	V_{PPF}	32.0	33.0	34.0	V	See note 3
	t_{pw}	10.0		40	μs	
	t_r	53	66	88	μs	See note 4
	t_f					N.A.
	Reject		27		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.1	4.2	4.3	V	
	V_{REF}	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	17.3	18.3	19.3	V	701-1998/TP2
	LOW LOAD	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.9	6.0	6.1	V	
	V_{REF}	2.9	3.0	3.1	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	5.2	5.7	6.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family D1.*
2. *Load RAM with hex 01 for Family D2.*
3. *V_{PP} starts at 25V and increments to 33V in 1-volt steps with 3 pulses per step.*
4. *TR is measured 10% to 90% of greatest amplitude $\overline{E_2}$ pulse.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTS	3/84

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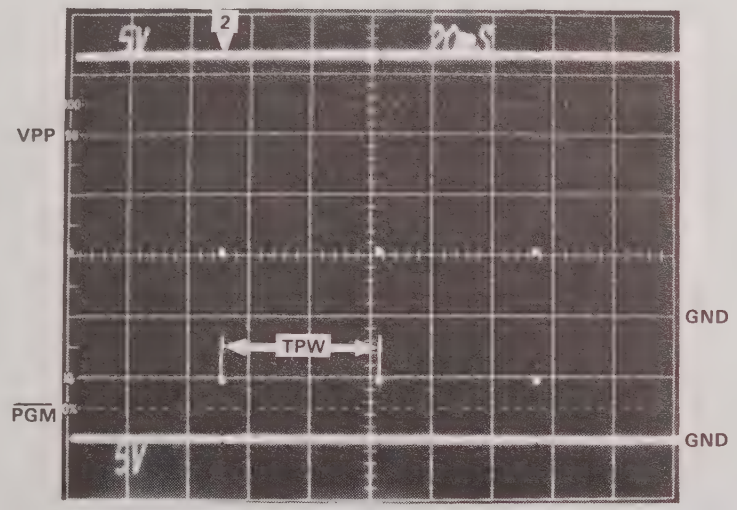
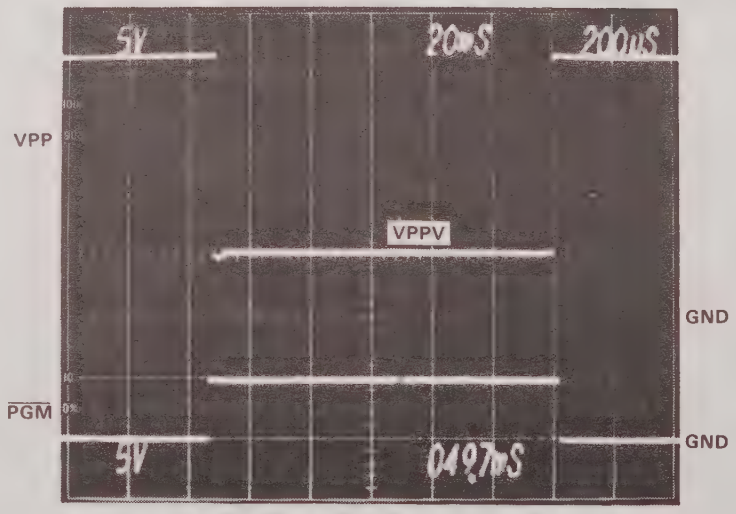
TIMING DIAGRAM

FAMILY CODES D1, D2

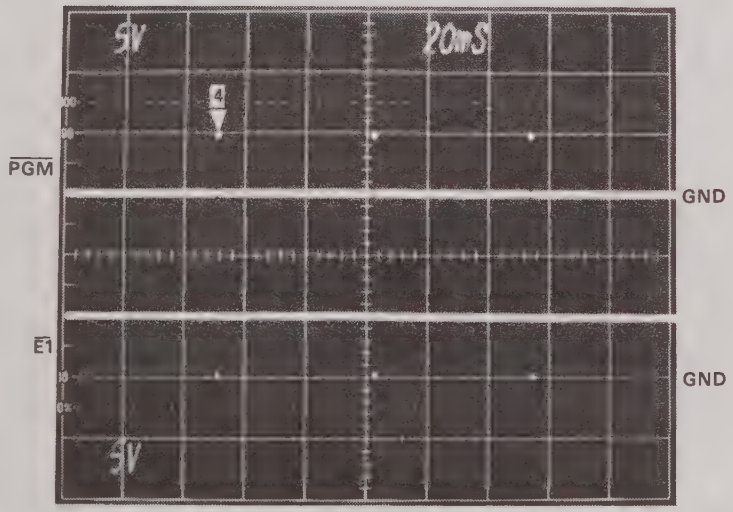
DATA I/O


5V
2
20mS
VPP
GND
TPW
PGM
GND
5V

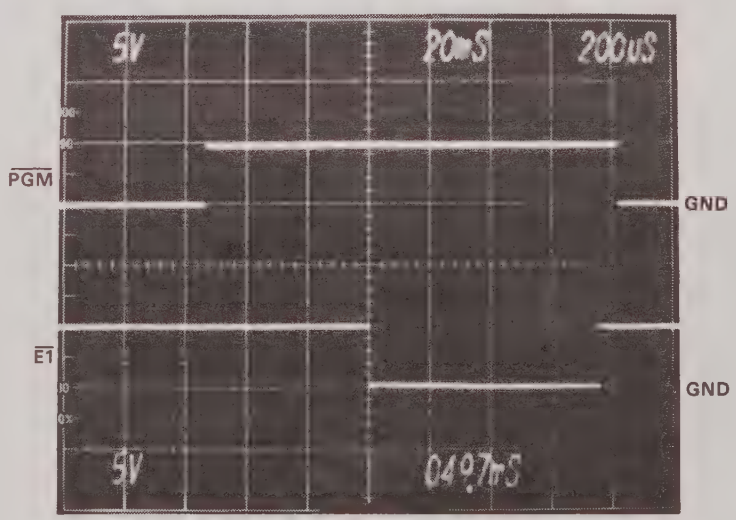
1


5V
20mS
200uS
VPP
VPPV
GND
PGM
GND
5V
049.7mS

2


5V
20mS
4
PGM
GND
E1
GND
5V

3


5V
20mS
200uS
PGM
GND
E1
GND
5V
049.7mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not shown
	VOP					N.A.
	VPP	20.5	21.0	21.5	V	
	VPPV	4.75	5.0	5.25	V	
	TPW	49.0	50.0	51.0	ms	
	TR					N.A.
	TF					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family 53.*
2. *Load RAM with hex 01 for Family 54 and bit-to-prog waveform becomes bit-no-prog waveform.*

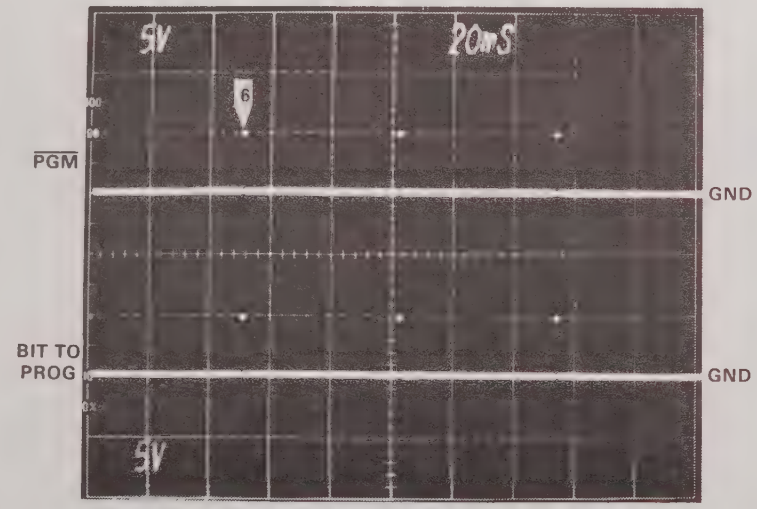
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

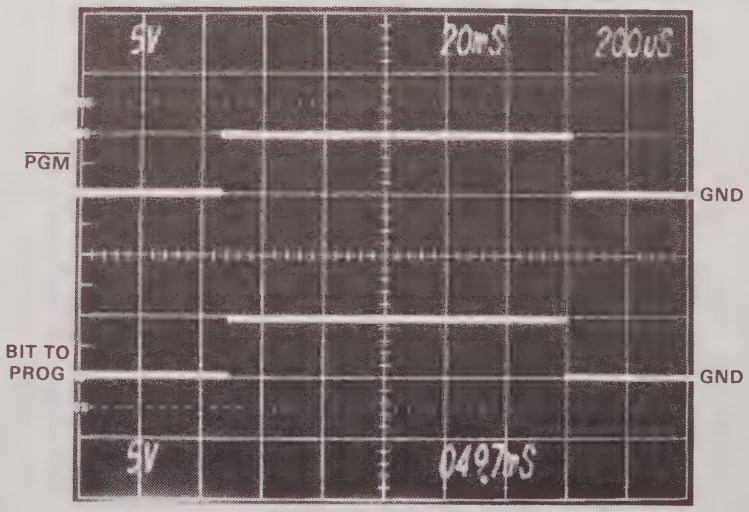
TIMING DIAGRAM

FAMILY CODES D5, D6

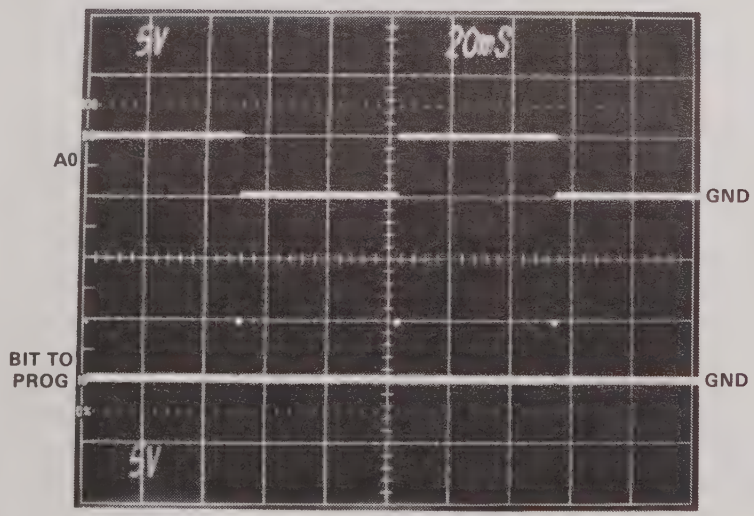
DATA I/O


5V
20mS
6
PGM
GND
BIT TO PROG
GND
5V

5


5V
20mS
200uS
PGM
GND
BIT TO PROG
GND
5V
049.7mS

6


5V
20mS
A0
GND
BIT TO PROG
GND
5V

7

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CJJ	7/14

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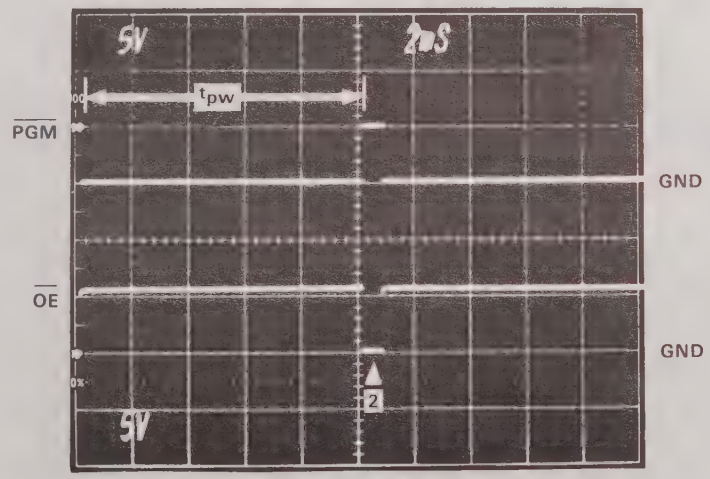
TIMING DIAGRAM

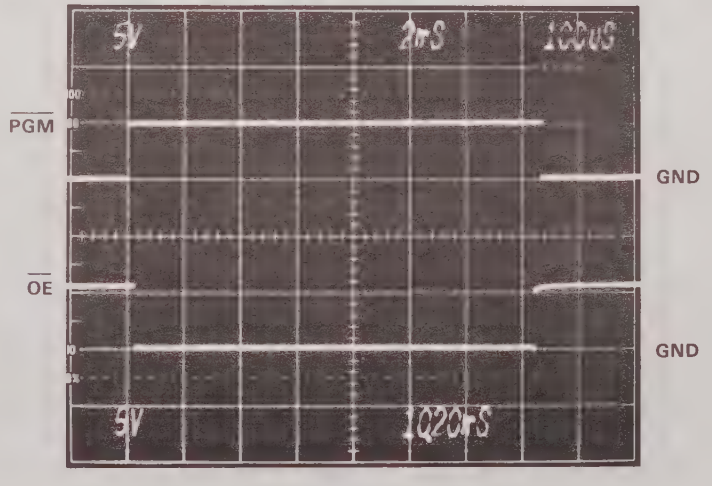
FAMILY CODES D5, D6

DATA I/O

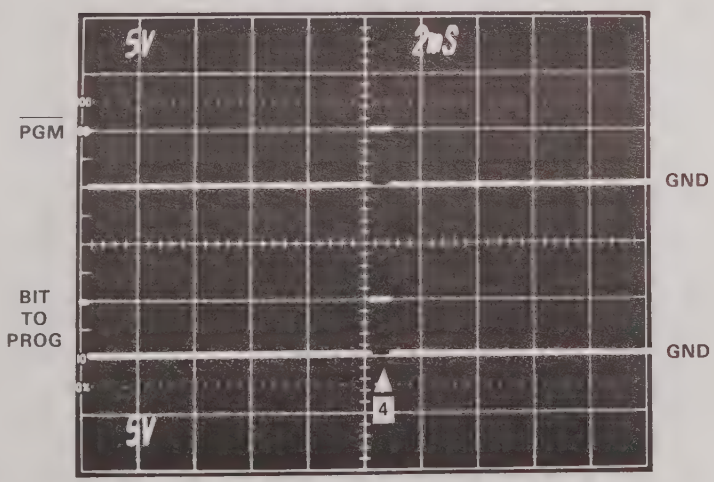
0526-1282


5V
2mS
t_{pw}
PGM
GND
OE
GND
2
5V

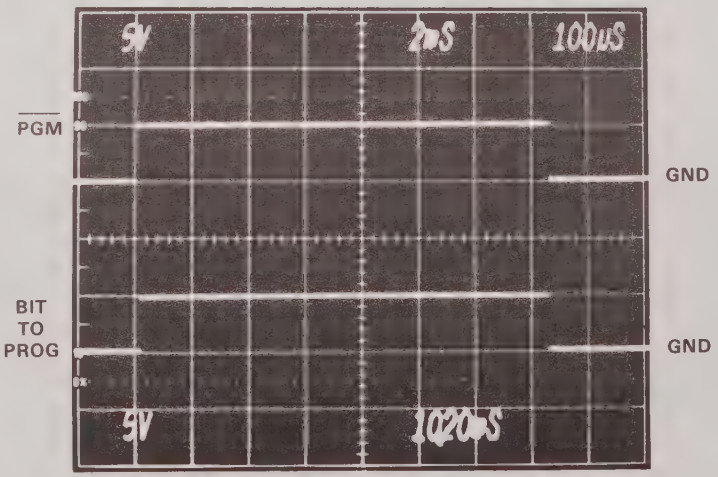
1


5V
2mS
100uS
PGM
GND
OE
GND
5V
1020mS

2


5V
2mS
PGM
GND
BIT
TO
PROG
GND
4
5V

3


5V
2mS
100uS
PGM
GND
BIT
TO
PROG
GND
5V
1020mS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					
	t_{pw}	9.5	10.0	10.5	ms	
	t_r					N.A.
	t_{ew}	95	100	105	ms	
	t_f					N.A.
	Reject		1		PULSE	
	Overprogram		0		PULSE	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family D7.*
2. *Load RAM with hex 01 for Family D8.*
3. *Photo 6 shows chip erase.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

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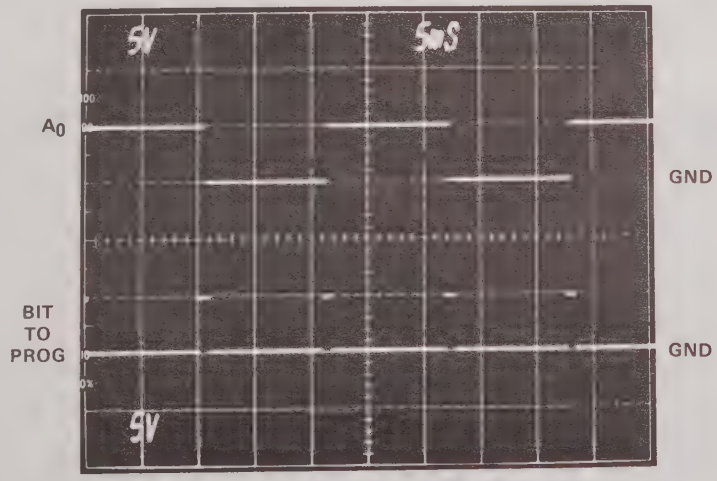
TIMING DIAGRAM

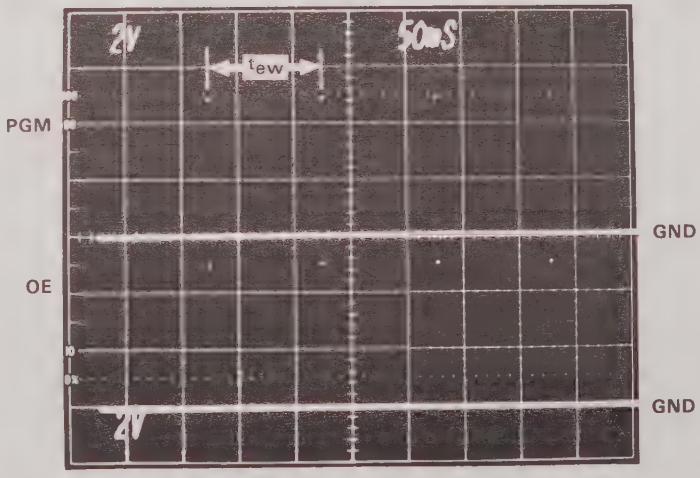
FAMILY CODES D7, D8

DATA I/O

0526/1282



5



6

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981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

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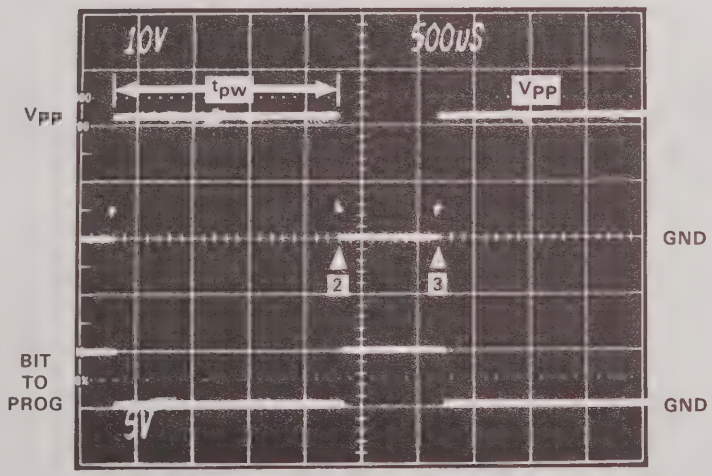
TIMING DIAGRAM

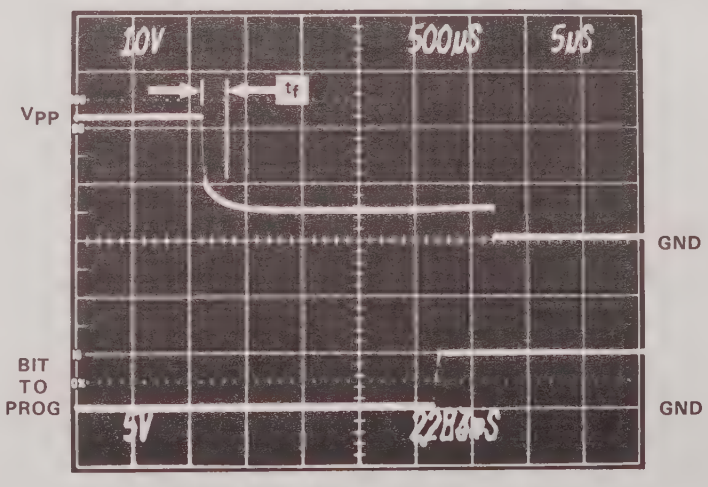
FAMILY CODES D7, D8

DATA I/O

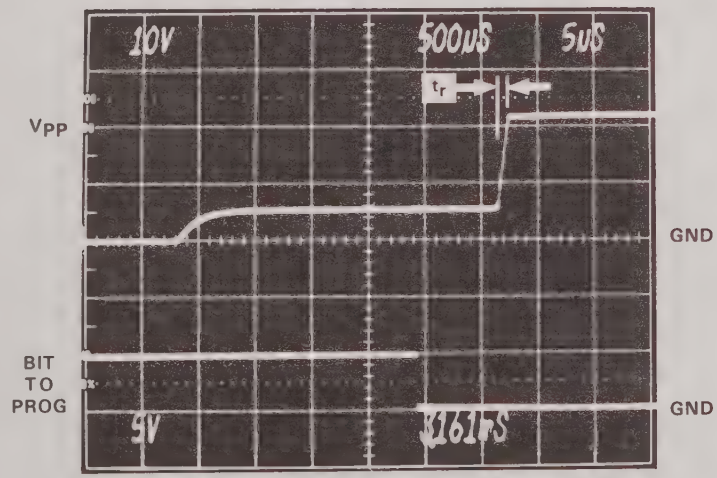
0526/1282


10V
500uS
tpw
VPP
VPP
GND
2
3
BIT
TO
PROG
5V
GND

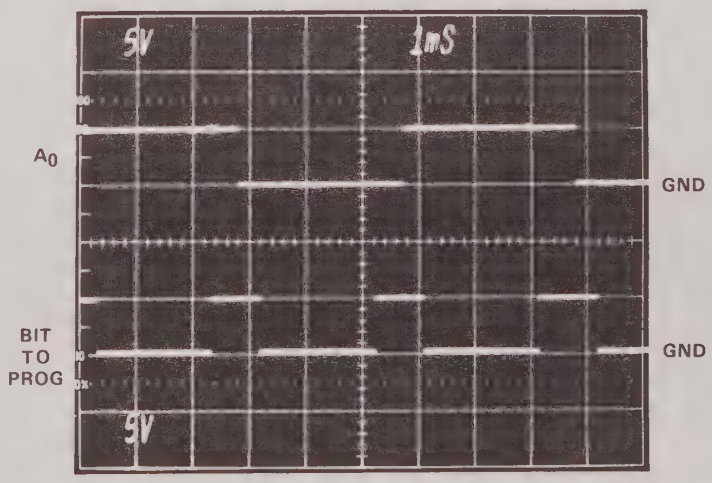
1


10V
500uS
5uS
tf
VPP
GND
BIT
TO
PROG
5V
GND

2


10V
500uS
5uS
tr
VPP
GND
BIT
TO
PROG
5V
GND

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}	20.5	21.0	21.5	V	
	V_{PP}					N.A.
	V_{PPV}					
	t_{pw}	1.9	2.0	2.1	ms	
	t_r	0.5		2.0	μs	
	t_f	0.5		5.0	μs	
	Reject		20		PASSES	
	Overprogram		5		PASSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.4	0.5	0.6	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.2	22.2	23.2	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.3	2.4	2.5	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. Load RAM with hex FE for Family D9
2. Load RAM with hex 01 for Family DA.

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LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

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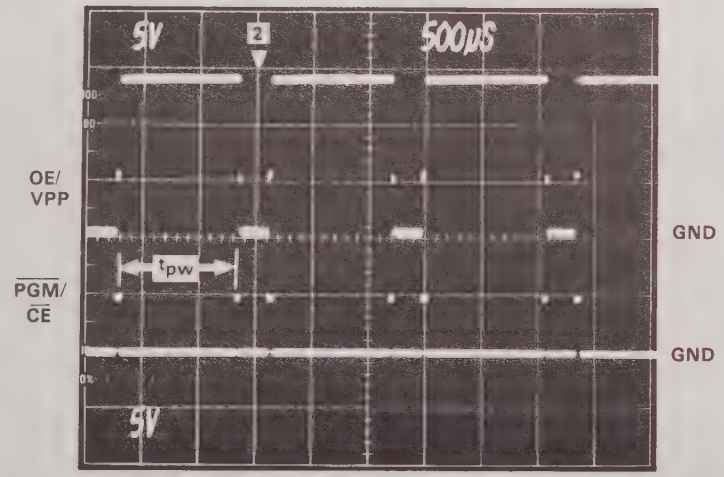
TIMING DIAGRAM

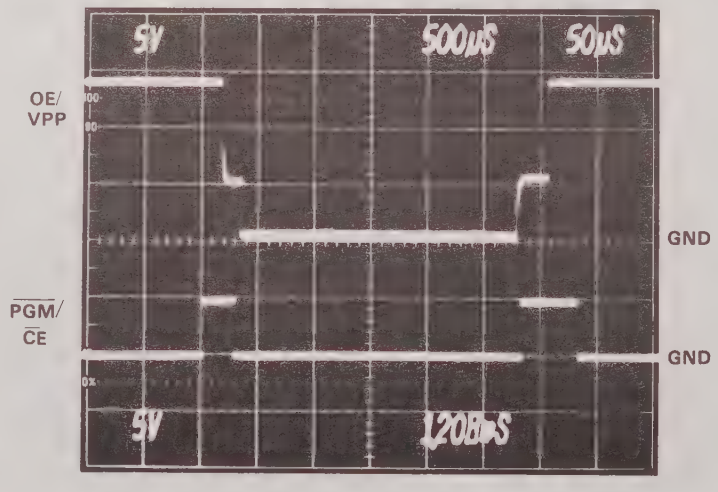
FAMILY CODES D9, DA

DATA I/O

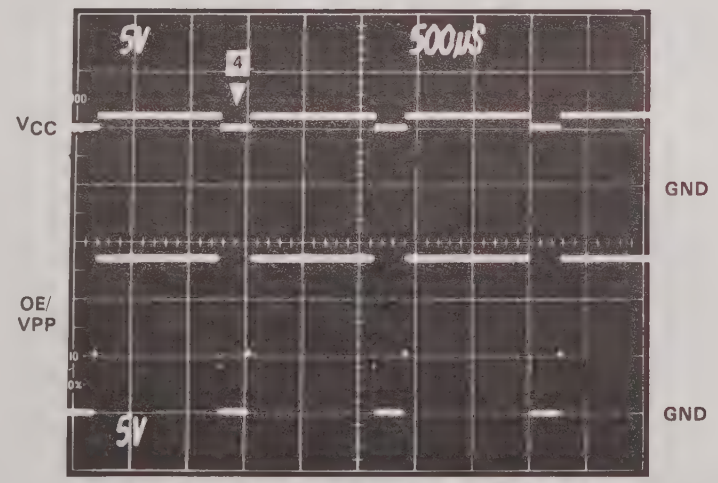
0526/1282


5V
2
500µS
OE/
VPP
GND
t_{pw}
PGM/
CE
GND
5V

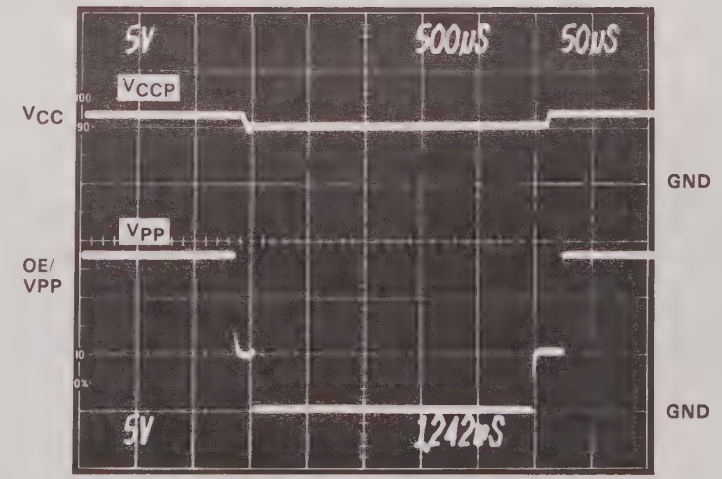
1


5V
500µS
50µS
OE/
VPP
GND
PGM/
CE
GND
5V
120µS

2


5V
4
500µS
VCC
GND
OE/
VPP
GND
5V

3


5V
500µS
50µS
VCCP
VCC
GND
VPP
OE/
VPP
GND
5V
1242µS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	5.75	6.0	6.25	V	
	V_{OP}					N.A.
	V_{PP}	12.5	13.0	13.5	V	
	V_{PPV}					N.A.
	t_{pw}	0.95	1	1.05	ms	
	t_r					N.A.
	t_f					N.A.
	Reject		25		PULSES	
	Overprogram		1		PULSES	
1ST PASS VERIFY	V_{CC}	4.7	4.8	4.9	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.1	5.2	5.3	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	4.4	4.9	5.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family DD.*
2. *Load RAM with hex 01 for Family DE.*

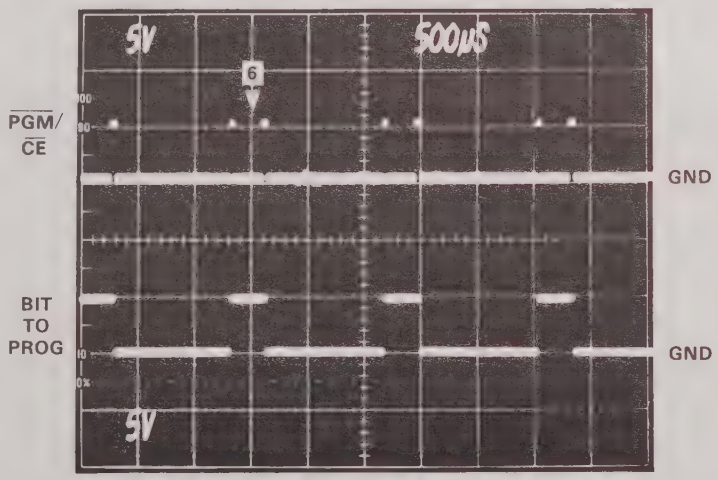
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTZ	3/84

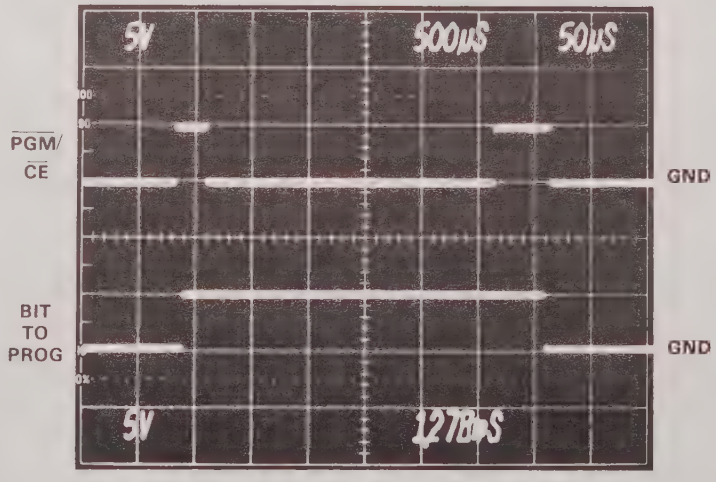
TIMING DIAGRAM

FAMILY CODES DD, DE

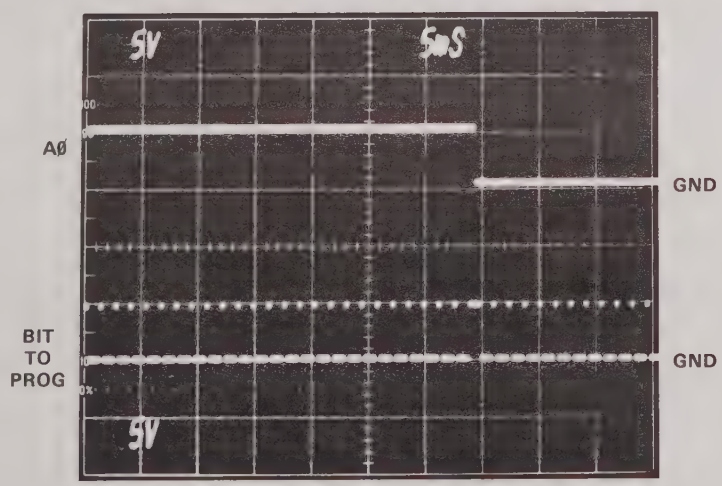
DATA I/O


5V
500µS
6
PGM/
CE
GND
BIT
TO
PROG
GND
5V

5


5V
500µS
50µS
PGM/
CE
GND
BIT
TO
PROG
GND
5V

6


5V
AØ
GND
BIT
TO
PROG
GND
5V

7

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981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

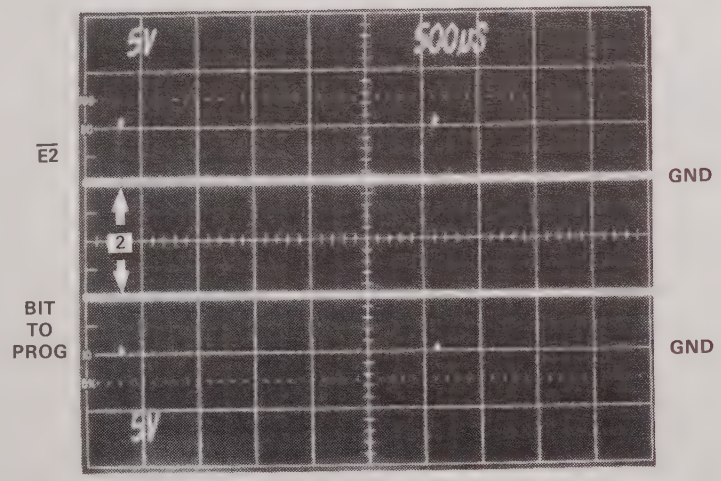
Sheet 2 of 2

TIMING DIAGRAM

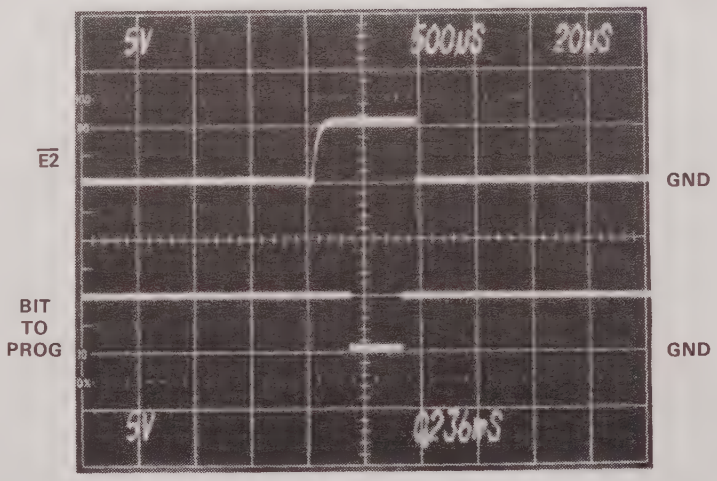
FAMILY CODES DD, DE

DATA I/O

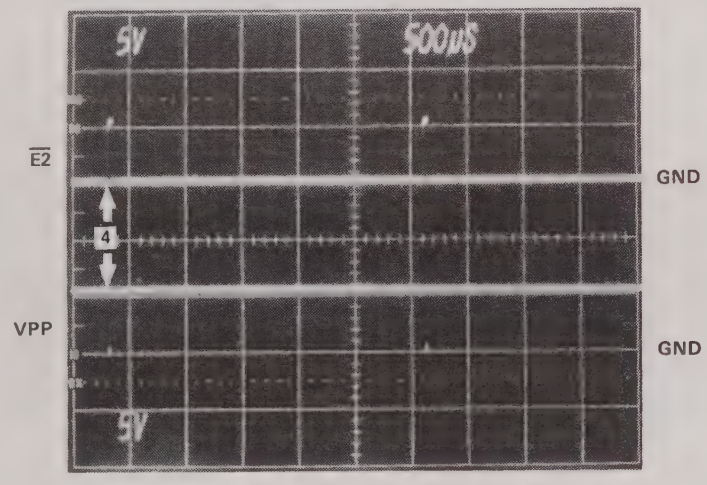
0526/1282


5V
500uS
E2
GND
2
BIT
TO
PROG
GND
5V

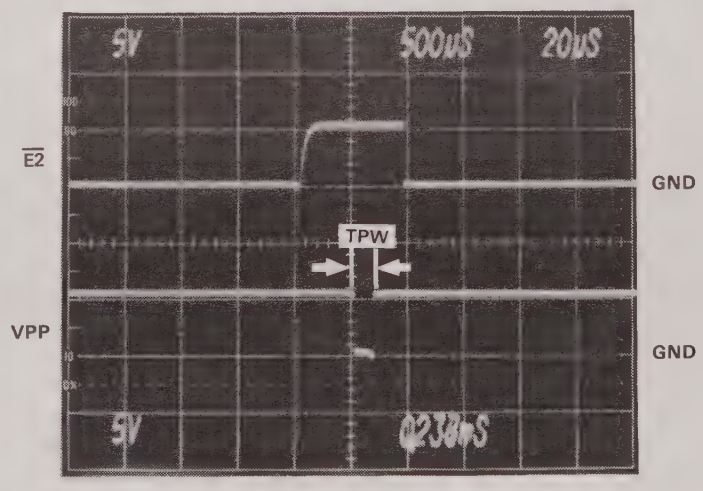
1


5V
500uS
20uS
E2
GND
BIT
TO
PROG
GND
5V
@236uS

2


5V
500uS
E2
GND
4
VPP
GND
5V

3


5V
500uS
20uS
E2
GND
TPW
VPP
GND
5V
@230uS

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VEP	20.5	21.0	21.5	V	
	VEE	11.5	12.0	12.5	V	
	TPW	150			ns	
	TEW	9.0		15.0	ms	
	Reject		1		Pulse	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.3	0.4	0.5	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	21.1	22.1	23.1	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.3	2.4	2.5	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	6.6	7.1	7.6	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family DF.*
2. *Load RAM with hex 01 for Family E0.*
3. *Photo 6 shows erase pulse.*

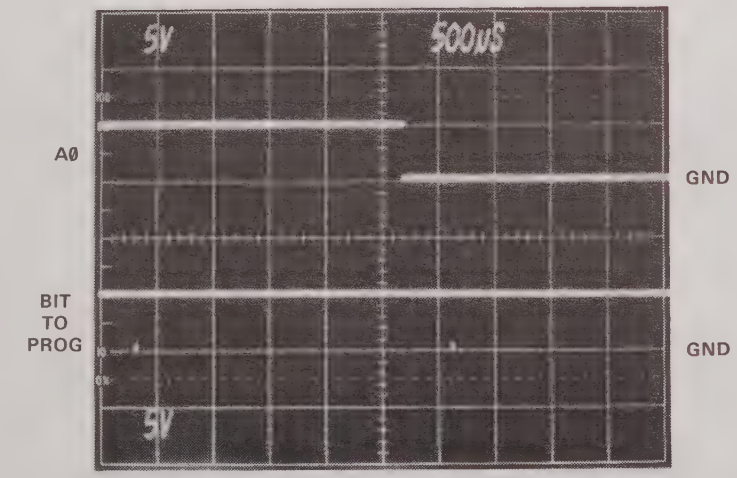
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

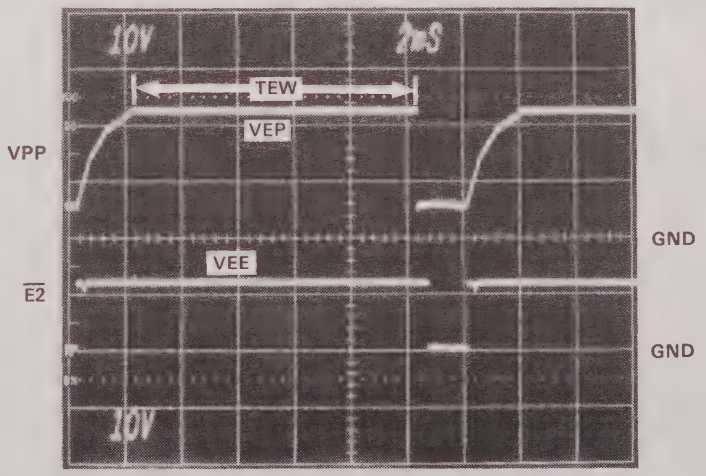
TIMING DIAGRAM

FAMILY CODES DF, E0

DATA I/O


5V
500uS
A0
GND
BIT
TO
PROG
GND
5V

5


10V
2mS
TEW
VEP
VPP
GND
VEE
$\overline{E2}$
GND
10V

6

B-239
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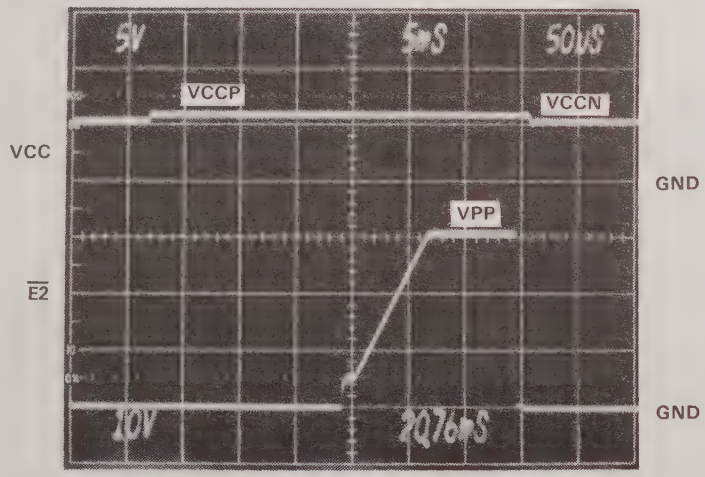
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

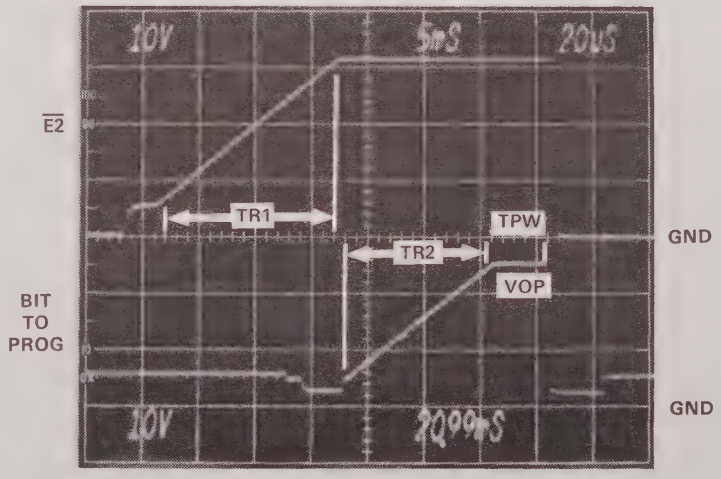
TIMING DIAGRAM

FAMILY CODES DF, E0

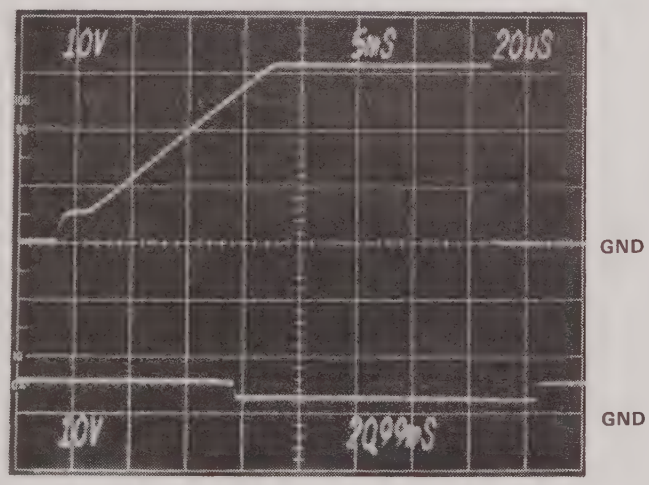
DATA I/O


5V
5mS
50uS
VCCP
VCCN
VCC
GND
VPP
E2
GND
10V
2Q76mS

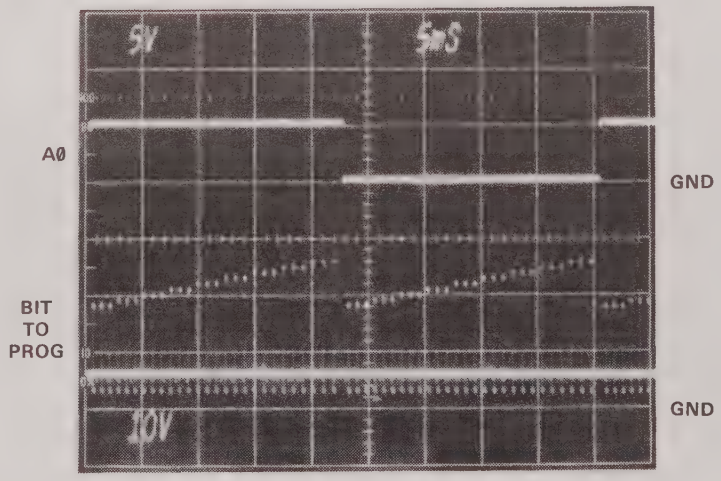
1


10V
5mS
20uS
E2
TR1
TPW
GND
TR2
VOP
BIT
TO
PROG
GND
10V
2Q99mS

2


10V
5mS
20uS
E2
GND
BIT
NO
PROG
GND
10V
2Q99mS

3


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.3	5.5	5.7	V	
	VCCN	4.75	5.0	5.25	V	
	VOPB	16.5	17.0	17.5	V	See Note 3
	VOPE	24.5	25.0	25.5	V	See Note 3
	VPPB	22.5	23.0	23.5	V	See Note 3
	VPPE	30.5	31.0	31.5	V	See Note 3
	TPW	10.0		40.0	μs	See Note 4
	TR1	50	63	82	μs	See Note 5
	TR2	40	50	66	μs	See Note 5
	Reject		27		Pulses	
	Overprogram		0		Pulses	
1ST PASS	VCC	4.1	4.2	4.3	V	
VERIFY	VREF	0.8	0.9	1.0	V	701-1998/TP4
	High Load	17.3	18.3	19.3	V	701-1998/TP2
	Low Load	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS	VCC	5.9	6.0	6.1	V	
VERIFY	VREF	2.9	3.0	3.1	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	4.7	5.7	6.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family E5.*
2. *Load RAM with hex 01 for Family E6.*
3. *These levels increment in 1-volt steps.*
4. *This is measured at the 90% level, and all nine pulse levels must meet this spec.*
5. *This is measured from 10% to 90% of the tallest pulse.*

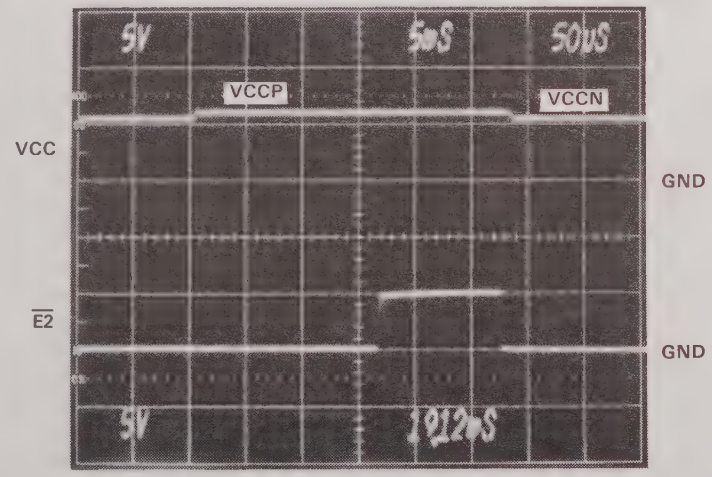
REVISIONS

LTR	DESCRIPTION	P.E.	DATE

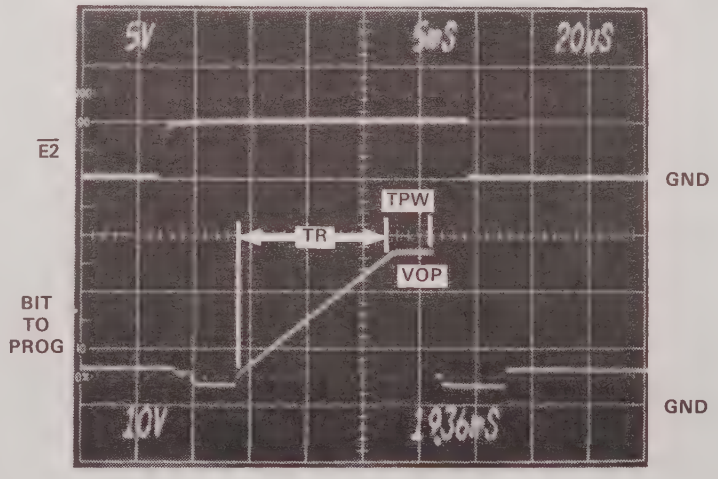
TIMING DIAGRAM

FAMILY CODES E5, E6

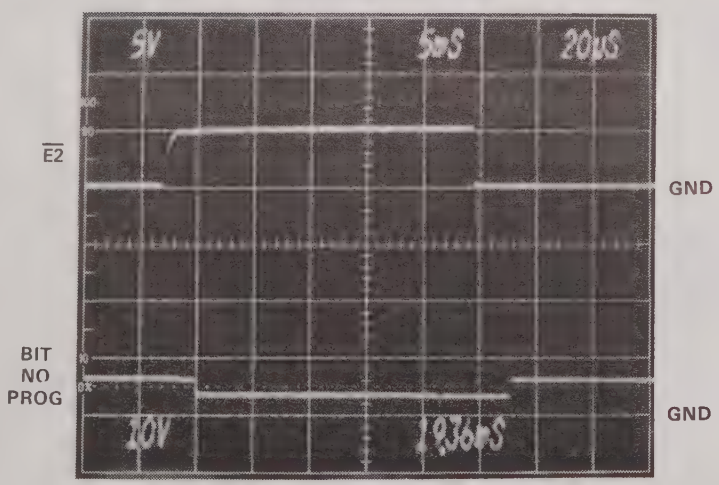
DATA I/O


5V
5mS
50µS
VCCP
VCCN
VCC
GND
$\overline{E2}$
GND
5V
1.212mS

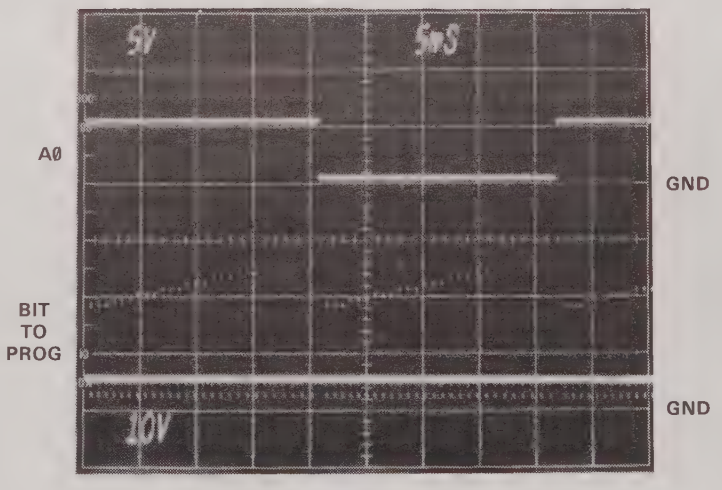
1


5V
5mS
20µS
$\overline{E2}$
GND
TPW
TR
VOP
BIT
TO
PROG
GND
10V
1.936mS

2


5V
5mS
20µS
$\overline{E2}$
GND
BIT
NO
PROG
GND
10V
1.936mS

3


5V
5mS
A0
GND
BIT
TO
PROG
GND
10V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	5.3	5.5	5.7	V	
	VCCN	4.75	5.0	5.25	V	
	VOPB	17.5	18.0	18.5	V	See Note 3
	VOPE	25.5	26.0	26.5	V	See Note 3
	TPW	10.0		40.0	μ	See Note 4
	TR	42	52	70	μ	See Note 5
	Reject		27		Pulses	
	Overprogram		0		Pulses	
1ST PASS VERIFY	VCC	4.1	4.2	4.3	V	
	VREF	0.8	0.9	1.0	V	701-1998/TP4
	High Load	17.3	18.3	19.3	V	701-1998/TP2
	Low Load	17.3	18.3	19.3	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1998/TP4
	High Load	0.0	0.0	0.4	V	701-1998/TP2
	Low Load	4.7	5.7	6.7	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family E7.*
2. *Load RAM with hex 01 for Family E8.*
3. *These levels incrememt in 1-volt steps.*
4. *This is measured at the 90% level, and all nine levels must meet this spec.*
5. *This is measured from 10% to 90% on the tallest pulse.*

REVISIONS

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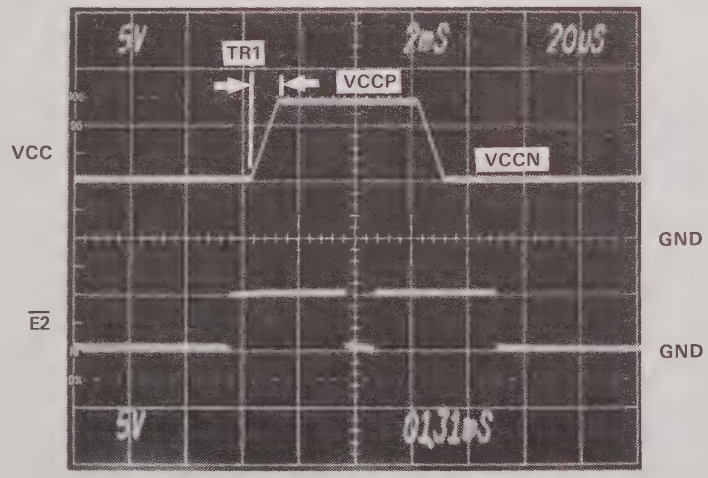
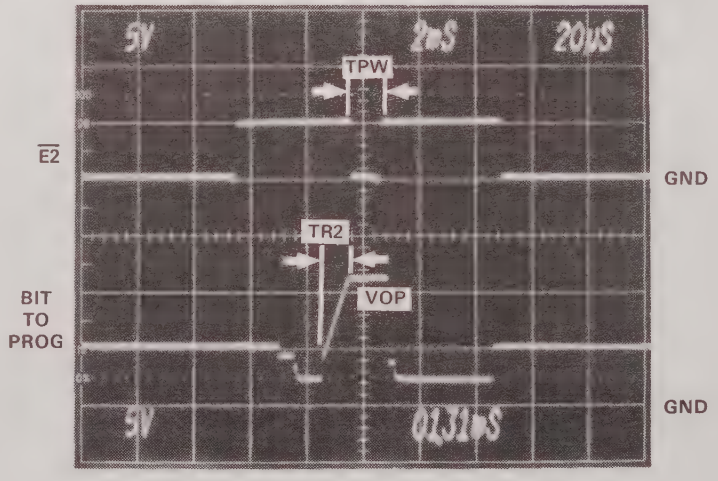
TIMING DIAGRAM

FAMILY CODES E7, E8

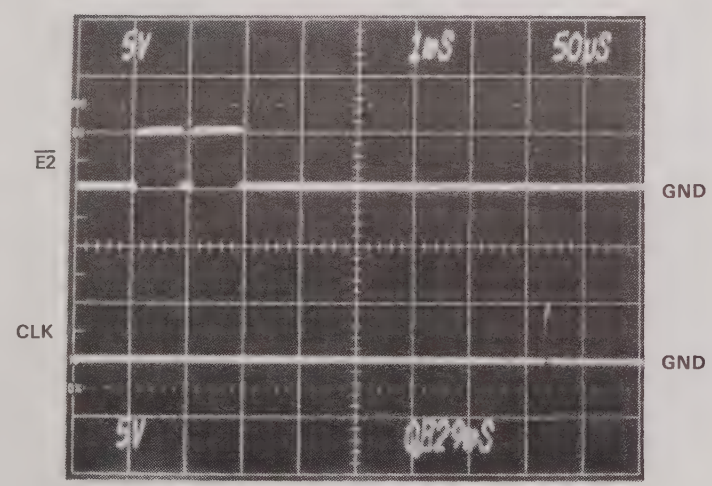
DATA I/O


5V
TR1
2mS
20uS
VCCP
VCC
VCCN
GND
E2
GND
5V
0131uS

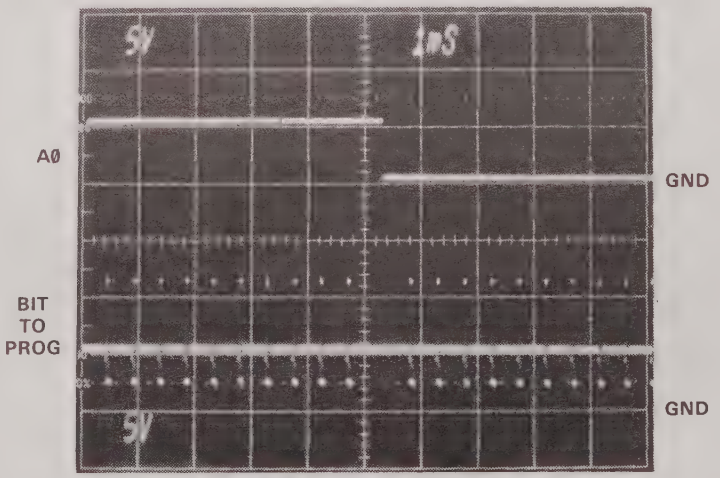
1


5V
2mS
20uS
TPW
E2
GND
TR2
BIT
TO
PROG
VOP
GND
5V
0131uS

2


5V
1mS
50uS
E2
GND
CLK
GND
5V

3


5V
1mS
A0
GND
BIT
TO
PROG
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	11.5	11.7	11.9	V	
	VCCN	4.75	5.0	5.25	V	
	VOP	10.5	11.0	11.5	V	
	TPW	9.0	10.0	11.0	μs	
	TR1	10.0		20.0	μs	See Note 3
	TR2	5.0		18.0	μs	
	Reject		10		Pulses	
	Overprogram		5		Pulses	
1ST PASS VERIFY	VCC	4.2	4.3	4.4	V	
	VREF	0.8	0.9	1.0	V	701-1998/TP4
	HIGH LOAD	6.4	7.4	8.4	V	701-1998/TP2
	LOW LOAD	6.4	7.4	8.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.9	6.0	6.1	V	
	VREF	2.9	3.0	3.1	V	701-1998/TP4
	High Load	7.2	8.2	9.2	V	701-1998/TP2
	Low Load	7.2	8.2	9.2	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family EB.*
2. *Load RAM with hex 01 for Family EC.*
3. *Load VCC with a 100Ω, 2-watt resistor.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

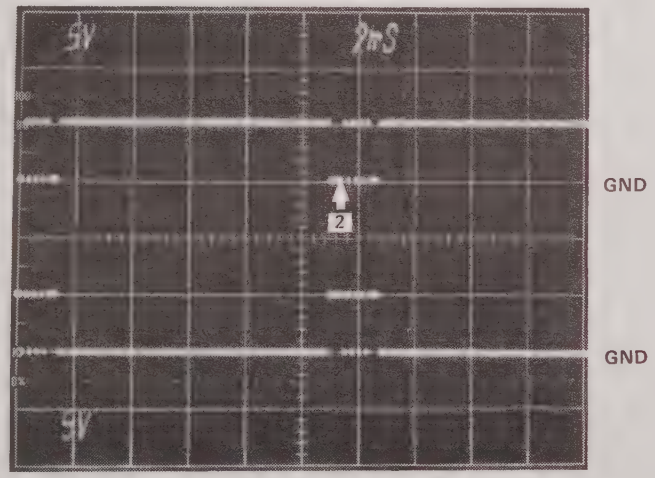
Sheet 1 of 1

TIMING DIAGRAM

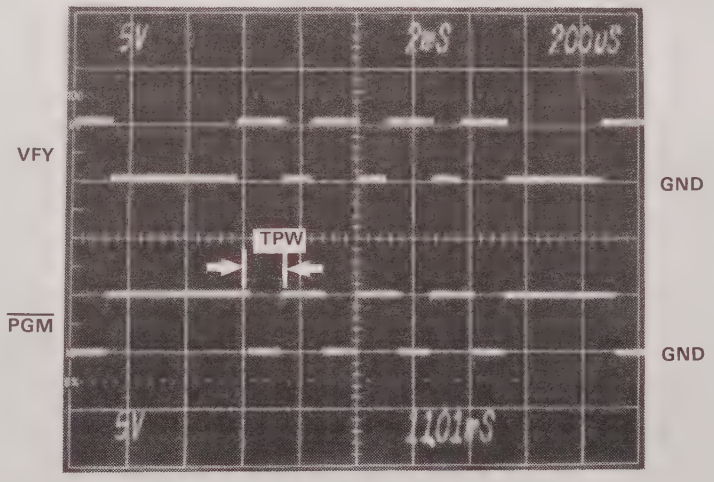
FAMILY CODES EB, EC

DATA I/O

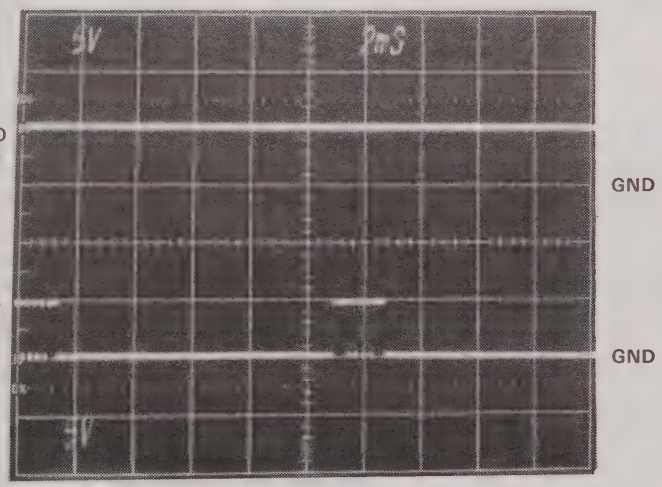
0526/1282


5V
2mS
VFY
GND
2
PGM
GND
5V

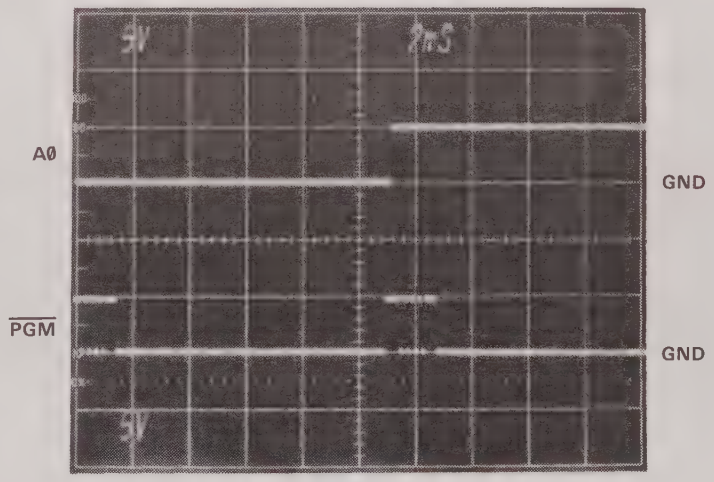
1


5V
2mS
200uS
VFY
GND
TPW
PGM
GND
5V

2


5V
2mS
BIT TO PROG "1"
GND
BIT TO PROG "0"
GND
5V

3


5V
2mS
A0
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	VCCP	4.75	5.0	5.25	V	Not Shown
	VPP	13.0	13.5	14.0	V	Not Shown
	TPW	95	100	105	μs	
	Reject		4		Pulses	
	Overprogram		1		Pulse	See Note 3
1ST PASS VERIFY	VCC	4.7	4.8	4.9	V	
	VREF	0.6	0.7	0.8	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	20.4	21.4	22.4	V	701-1998/TP3
2ND PASS VERIFY	VCC	5.1	5.2	5.3	V	
	VREF	2.1	2.2	2.3	V	701-1998/TP4
	High Load	0.0	0.0	0.5	V	701-1998/TP2
	Low Load	3.9	4.9	5.9	V	701-1998/TP3

NOTES

1. *Load RAM with hex 01 for both families.*
2. *Both zeros and ones have to be programmed.*
3. *The overprogram pulse is 2.4 ms times the number of programming pulses required to program the location.*

REVISIONS

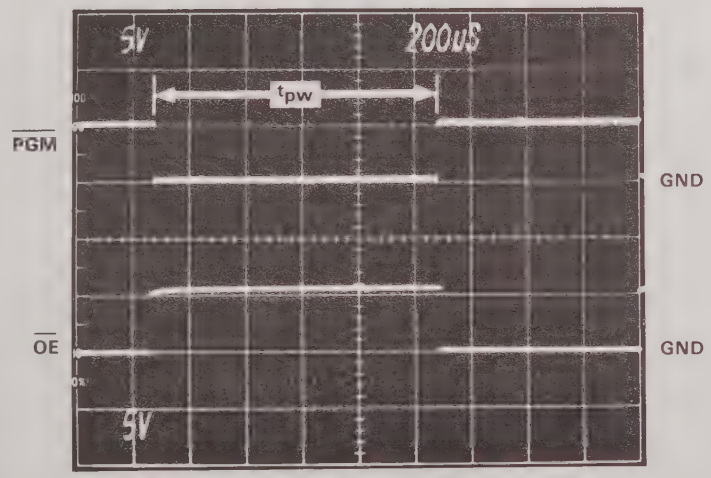
LTR	DESCRIPTION	P.E.	DATE

Sheet 1 of 1

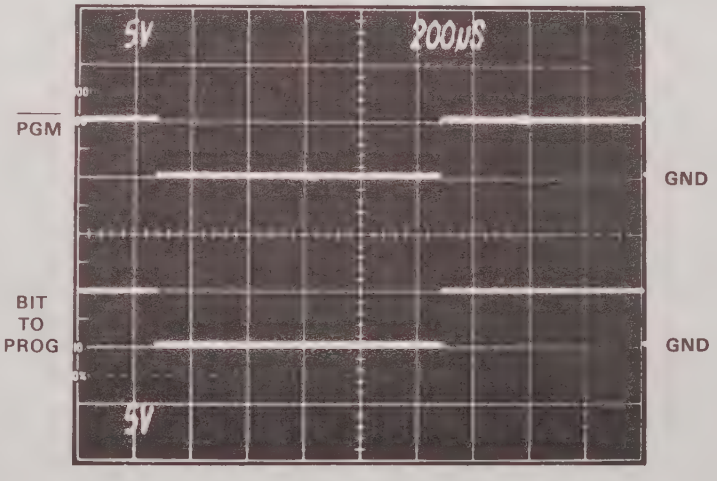
TIMING DIAGRAM

FAMILY CODES ED, EE

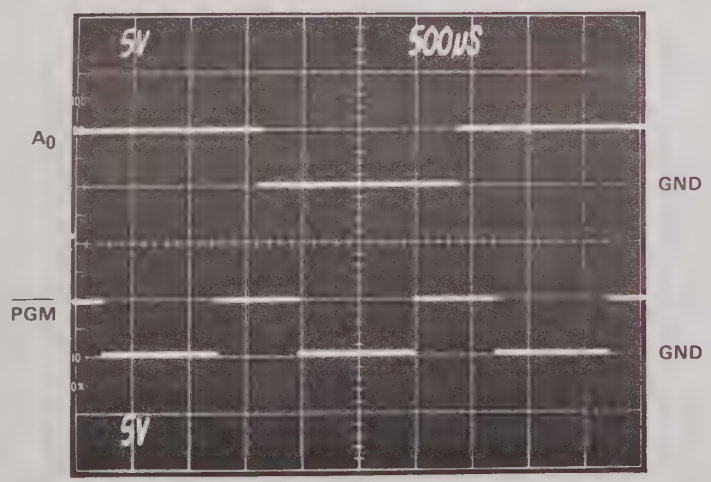
DATA I/O


5V
200uS
t_{pw}
PGM
GND
OE
GND
5V

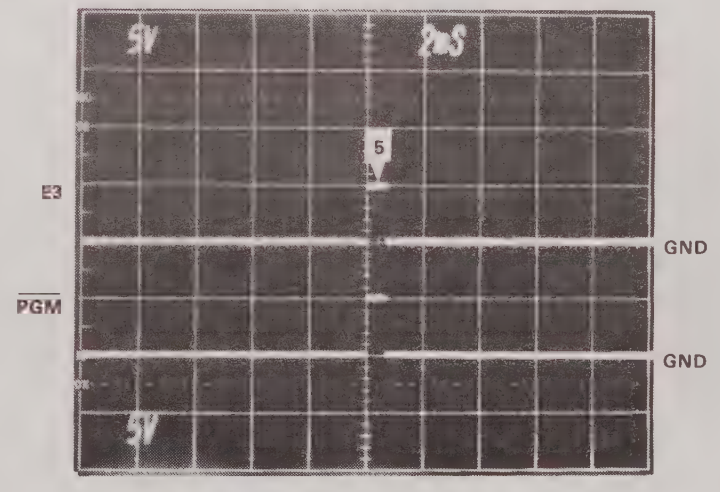
1


5V
200uS
PGM
GND
BIT
TO
PROG
GND
5V

2


5V
500uS
A_0
GND
PGM
GND
5V

3


5V
2mS
5
E3
GND
PGM
GND
5V

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CCP}	4.75	5.0	5.25	V	Not Shown
	V_{OP}					N.A.
	V_{PP}					N.A.
	V_{PPV}					N.A.
	t_{pw}	0.95	1.0	1.05	ms	
	t_r					N.A.
	t_{ew}	9.5	10.0	10.5	ms	
	t_f					N.A.
	Reject		1		Pulse	
	Overprogram		0		Pulse	
1ST PASS VERIFY	V_{CC}	4.5	4.6	4.7	V	
	V_{REF}	0.6	0.7	0.8	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	21.4	22.4	23.4	V	701-1998/TP3
2ND PASS VERIFY	V_{CC}	5.3	5.4	5.5	V	
	V_{REF}	2.1	2.2	2.3	V	701-1998/TP4
	HIGH LOAD	0.0	0.0	0.5	V	701-1998/TP2
	LOW LOAD	7.4	7.9	8.4	V	701-1998/TP3

NOTES

1. *Load RAM with hex FE for Family B9.*
2. *Photos 4-7 are chip-erase photos.*

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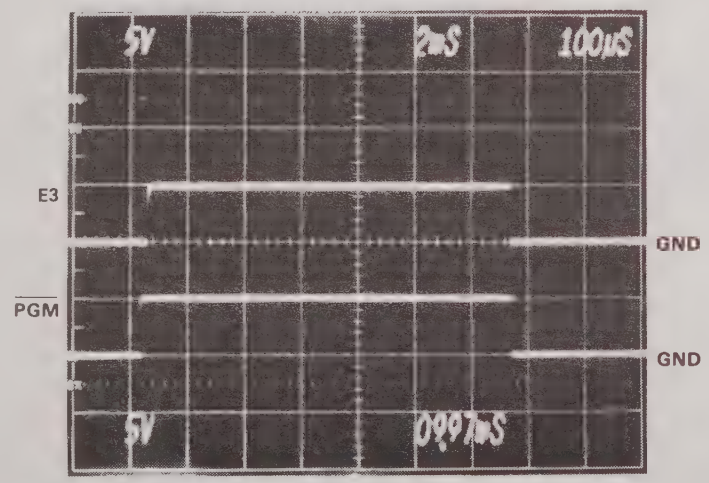
LTR	DESCRIPTION	P.E.	DATE
	ECN #5022	CTJ	3/84

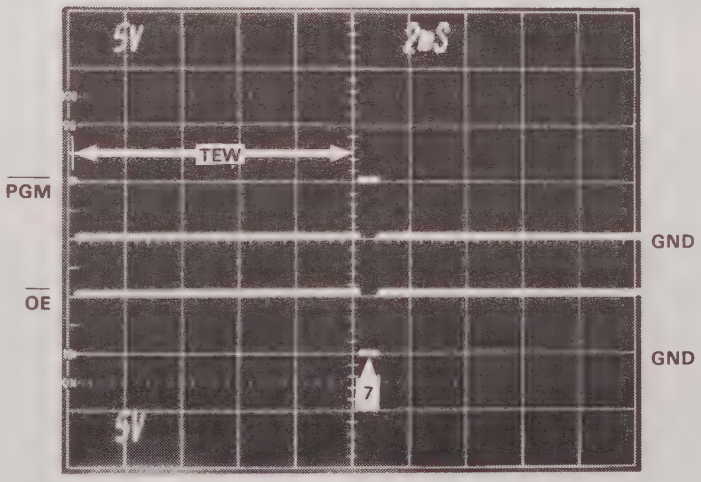
TIMING DIAGRAM

FAMILY CODES F1, F2

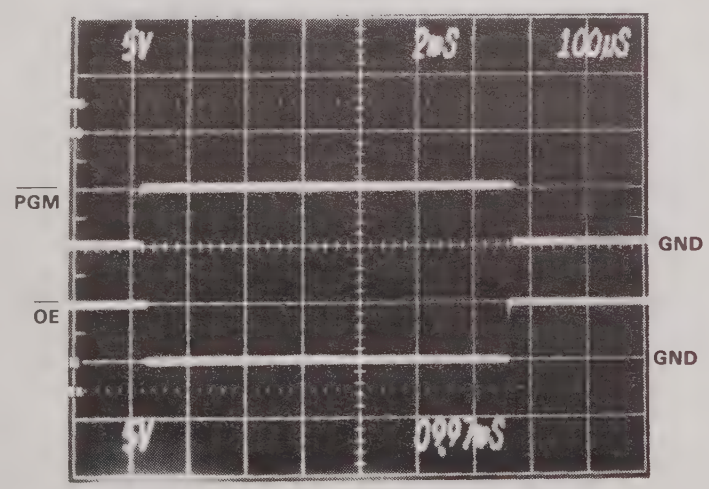
DATA I/O


5V
2mS
100µS
E3
GND
PGM
GND
5V

5


5V
2mS
TEW
PGM
GND
OE
GND
7
5V

6


5V
2mS
100µS
PGM
GND
OE
GND
5V

7

B-251
981-0003

REVISIONS

LTR	DESCRIPTION	P.E.	DATE

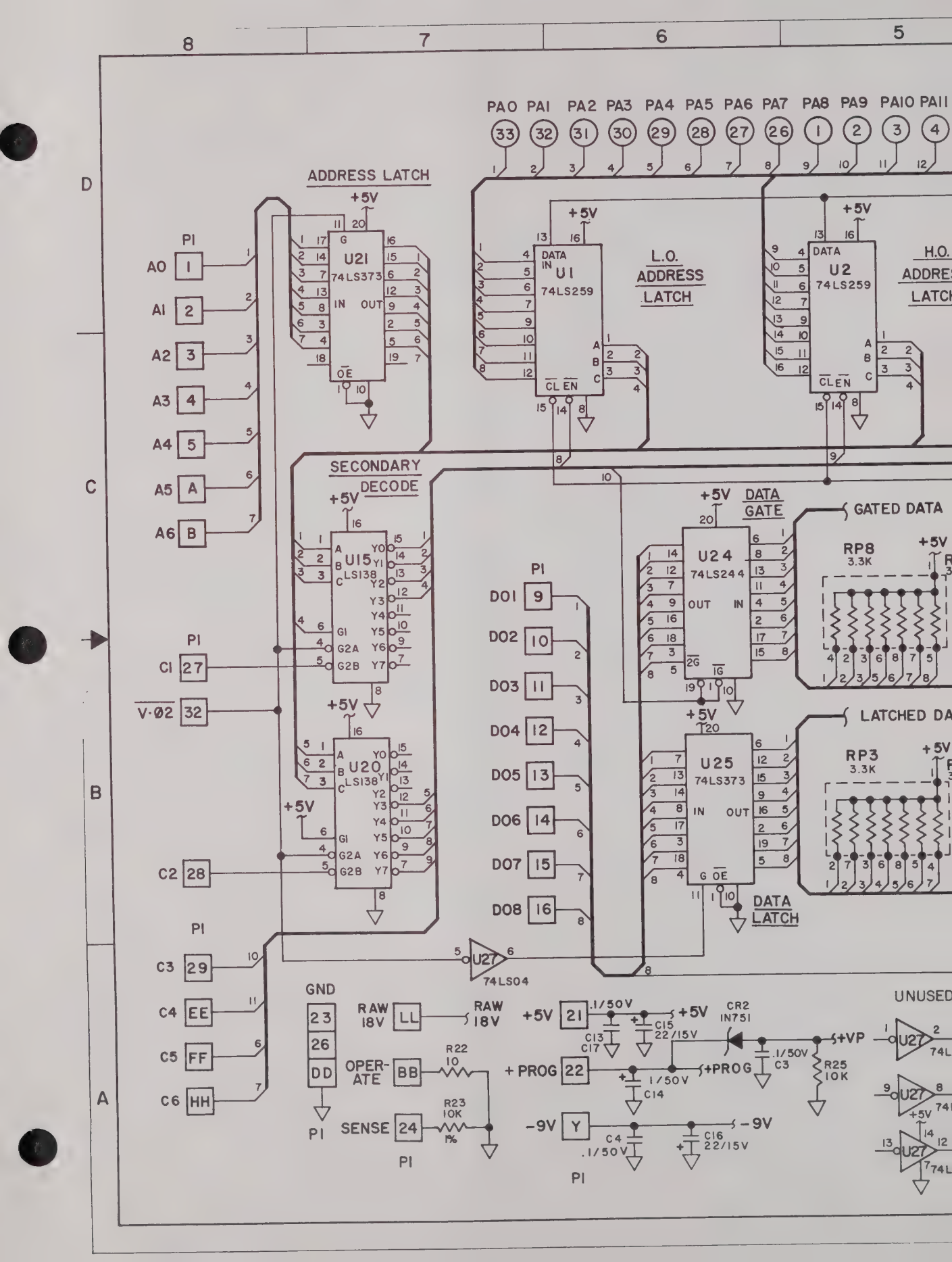
TIMING DIAGRAM

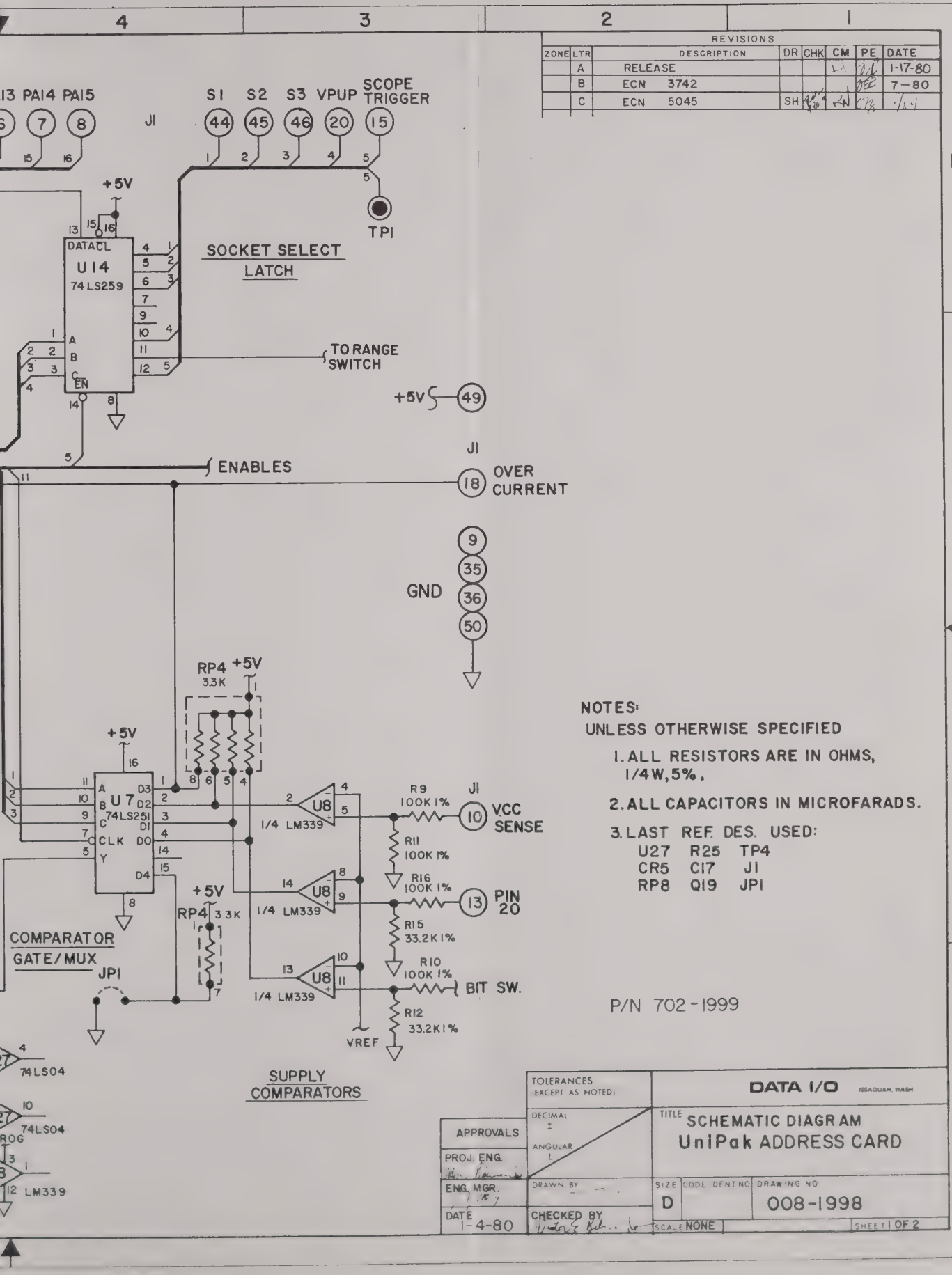
FAMILY CODES F1, F2

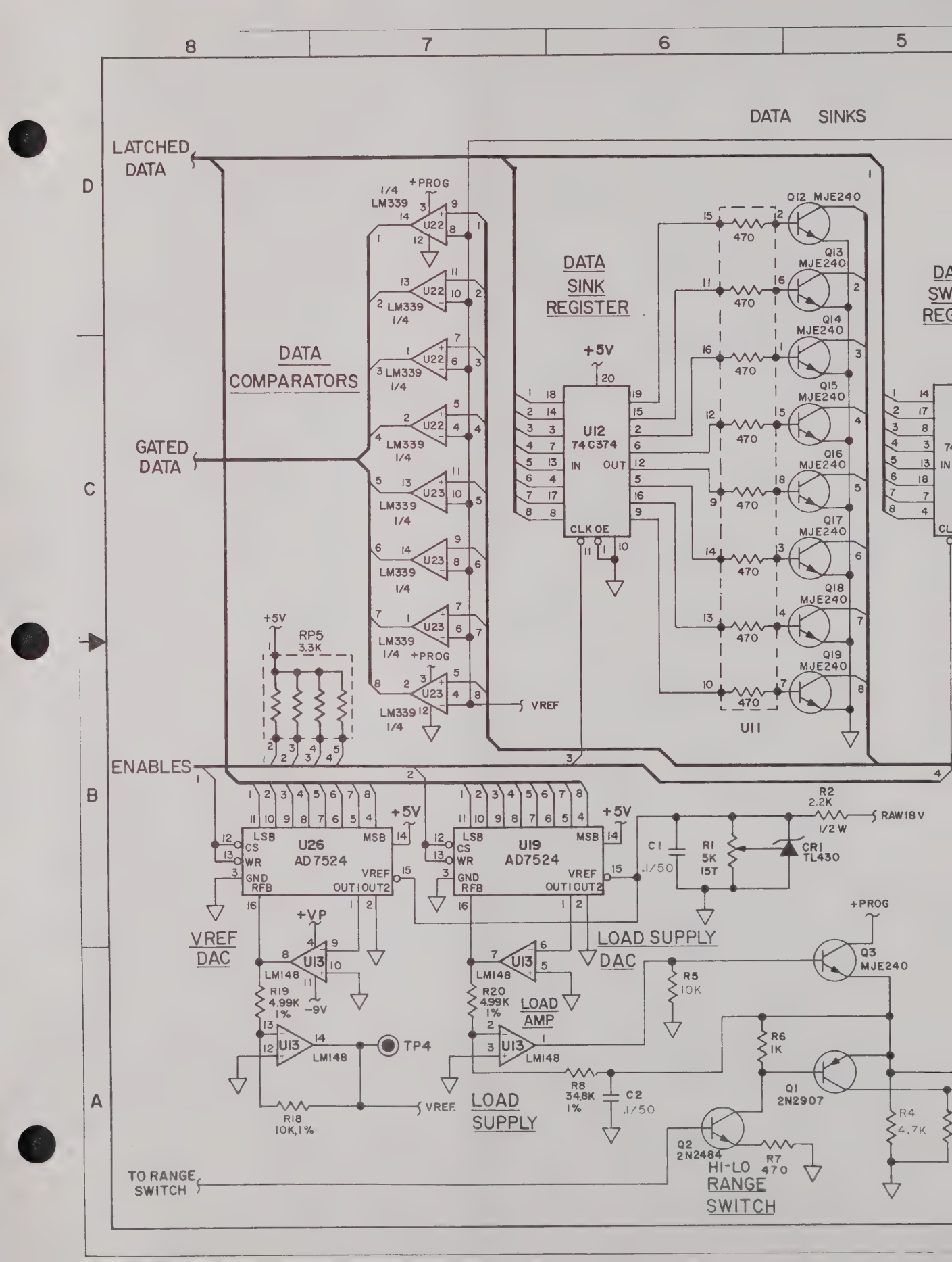
DATA I/O

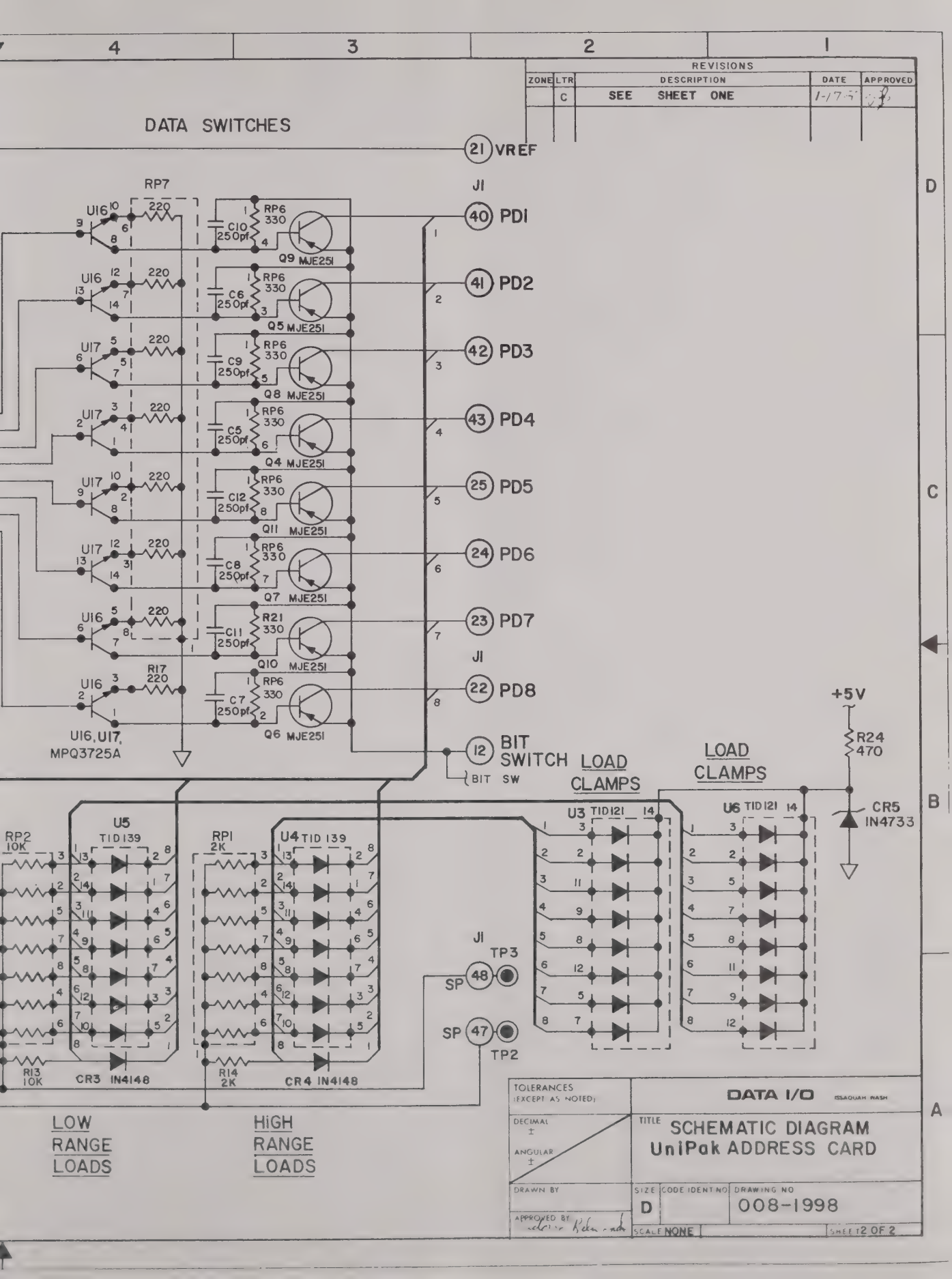
APPENDIX C
SCHEMATICS

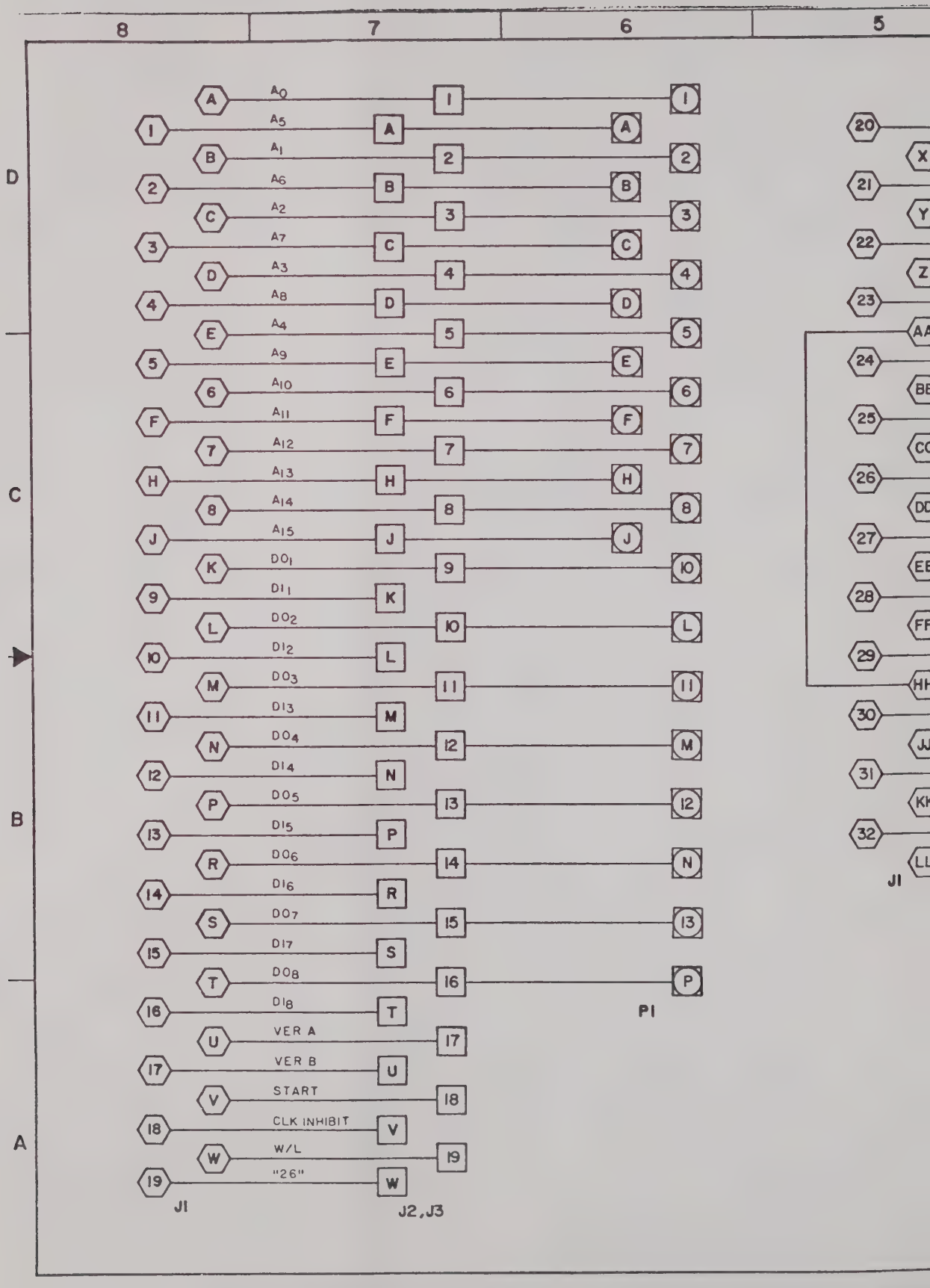
008-1998	Rev C	Address Card
008-1999	Rev A	Motherboard
30-701-7997	Rev B	Waveform Generator
30-702-0045	Rev B	UniPak™ Memory
30-702-7995	Rev B	Socket Assembly

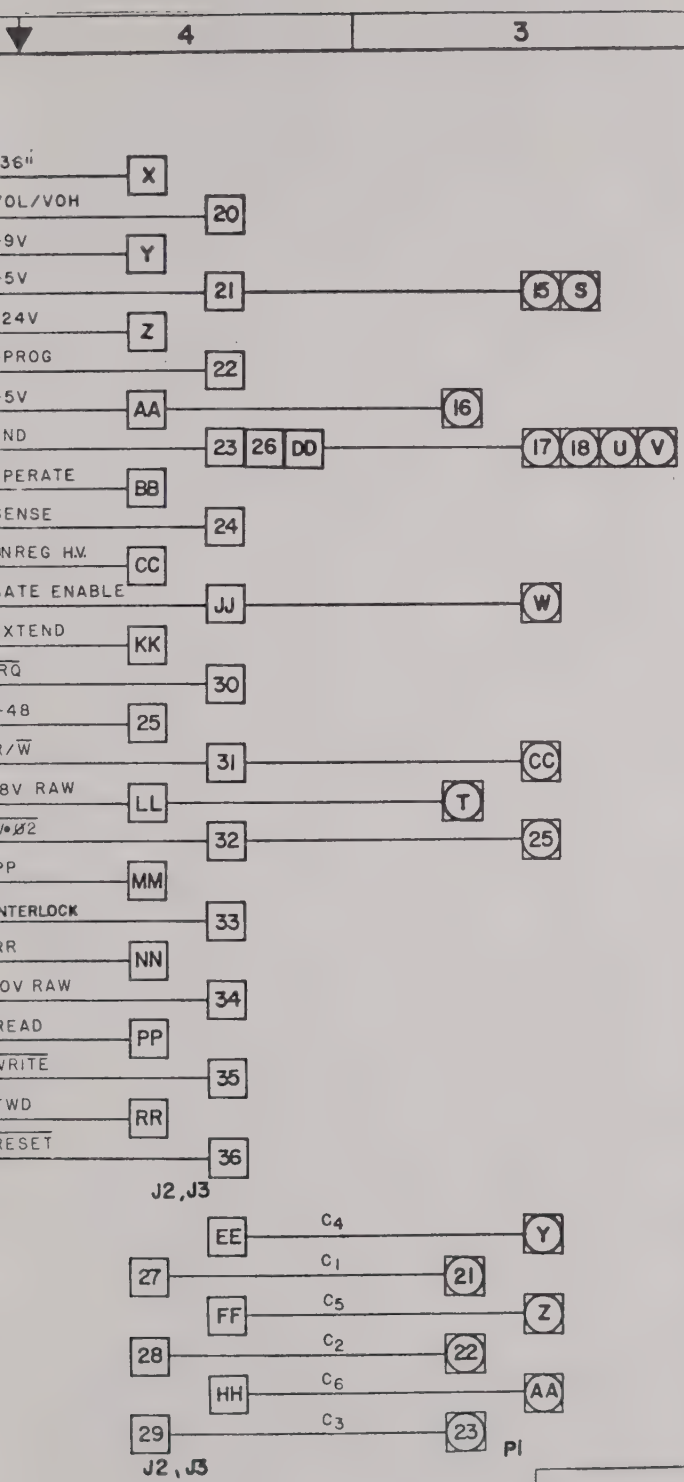

8
7
6
5
D
C
B
A
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7 PA8 PA9 PA10 PA11
33 32 31 30 29 28 27 26 1 2 3 4
ADDRESS LATCH
+5V
U21
74LS373
IN OUT
OE
P1
A0 1
A1 2
A2 3
A3 4
A4 5
A5 A 6
A6 B 7
U1
74LS259
DATA IN
CL EN
L.O. ADDRESS LATCH
U2
74LS259
H.O. ADDRESS LATCH
SECONDARY DECODE
U15
LS138
U20
LS138
G1 G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
C1 27
V·Ø2 32
C2 28
C3 29
C4 EE
C5 FF
C6 HH
DO1 9
DO2 10
DO3 11
DO4 12
DO5 13
DO6 14
DO7 15
DO8 16
DATA GATE
U24
74LS244
OUT IN
GATED DATA
RP8
3.3K
U25
74LS373
IN OUT
G OE
DATA LATCH
LATCHED DA
RP3
3.3K
U27
74LS04
GND
23 26 DD
RAW 18V LL
OPER-ATE BB
R22 10
SENSE 24
R23 10K 1%
+5V 21
.1/50V
C13 C17
C15 22/15V
CR2 IN751
+VP
+PROG 22
C14
C3
R25 10K
-9V Y
C4 .1/50V
C16 22/15V
UNUSED


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION DR CHK CM PE DATE
A RELEASE 1-17-80
B ECN 3742 7-80
C ECN 5045
D
C
B
A
PAI4 PAI5
J1
S1 S2 S3 VPUP SCOPE TRIGGER
+5V
TPI
SOCKET SELECT LATCH
U14
74LS259
DATA CL
EN
TO RANGE SWITCH
+5V
ENABLES
OVER CURRENT
GND
RP4 3.3K
U7
74LS251
CLK
U8
1/4 LM339
R9 100K 1%
R11 100K 1%
R16 100K 1%
R15 33.2K 1%
R10 100K 1%
R12 33.2K 1%
VCC SENSE
PIN 20
BIT SW.
VREF
COMPARATOR GATE/MUX
JP1
SUPPLY COMPARATORS
74LS04
LM339
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS IN MICROFARADS.
3. LAST REF. DES. USED:
U27 R25 TP4
CR5 C17 J1
RP8 Q19 JP1
P/N 702-1999
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
ANGULAR ±
APPROVALS
PROJ. ENG.
ENG. MGR.
DATE 1-4-80
DRAWN BY
CHECKED BY
DATA I/O ISSAQUAH, WASH
TITLE SCHEMATIC DIAGRAM UniPak ADDRESS CARD
SIZE D
CODE IDENT NO
DRAWING NO 008-1998
SCALE NONE
SHEET 1 OF 2

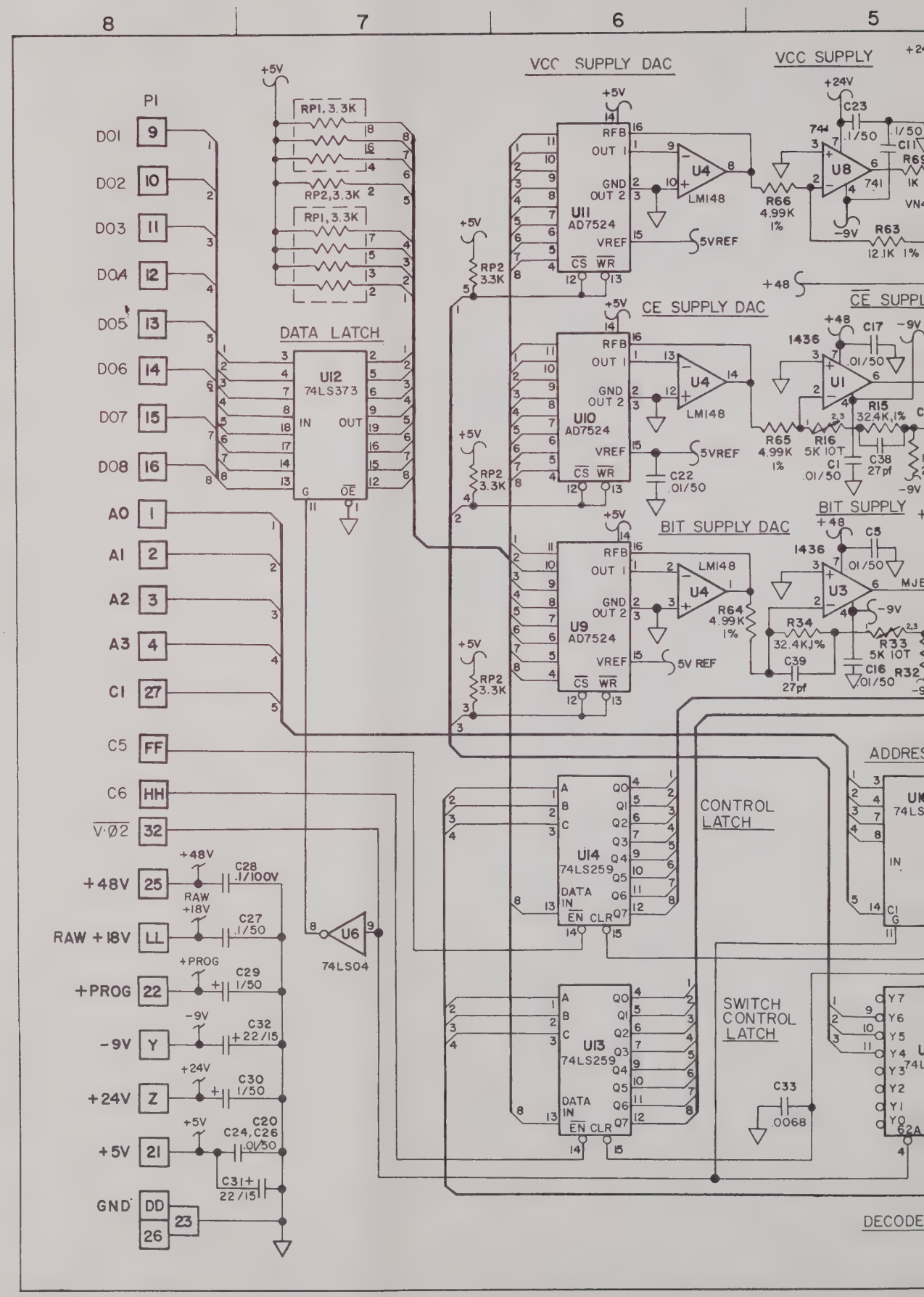

8
7
6
5
D
C
B
A
DATA SINKS
LATCHED DATA
GATED DATA
ENABLES
DATA COMPARATORS
DATA SINK REGISTER
+PROG
1/4 LM339
U22
U23
+5V
RP5 3.3K
VREF
U12 74C374
IN OUT
CLK OE
Q12 MJE240
Q13 MJE240
Q14 MJE240
Q15 MJE240
Q16 MJE240
Q17 MJE240
Q18 MJE240
Q19 MJE240
470
U11
U26 AD7524
U19 AD7524
LSB MSB
CS WR
GND RFB
VREF OUT1 OUT2
+VP
U13 LM148
-9V
R19 4.99K 1%
R20 4.99K 1%
R18 10K,1%
TP4
VREF DAC
LOAD SUPPLY DAC
LOAD AMP
LOAD SUPPLY
R2 2.2K 1/2W
RAW18V
C1 .1/50
R1 5K 15T
CR1 TL430
R5 10K
Q3 MJE240
R6 1K
Q1 2N2907
R4 4.7K
R8 34.8K 1%
C2 .1/50
Q2 2N2484
R7 470
HI-LO RANGE SWITCH
TO RANGE SWITCH

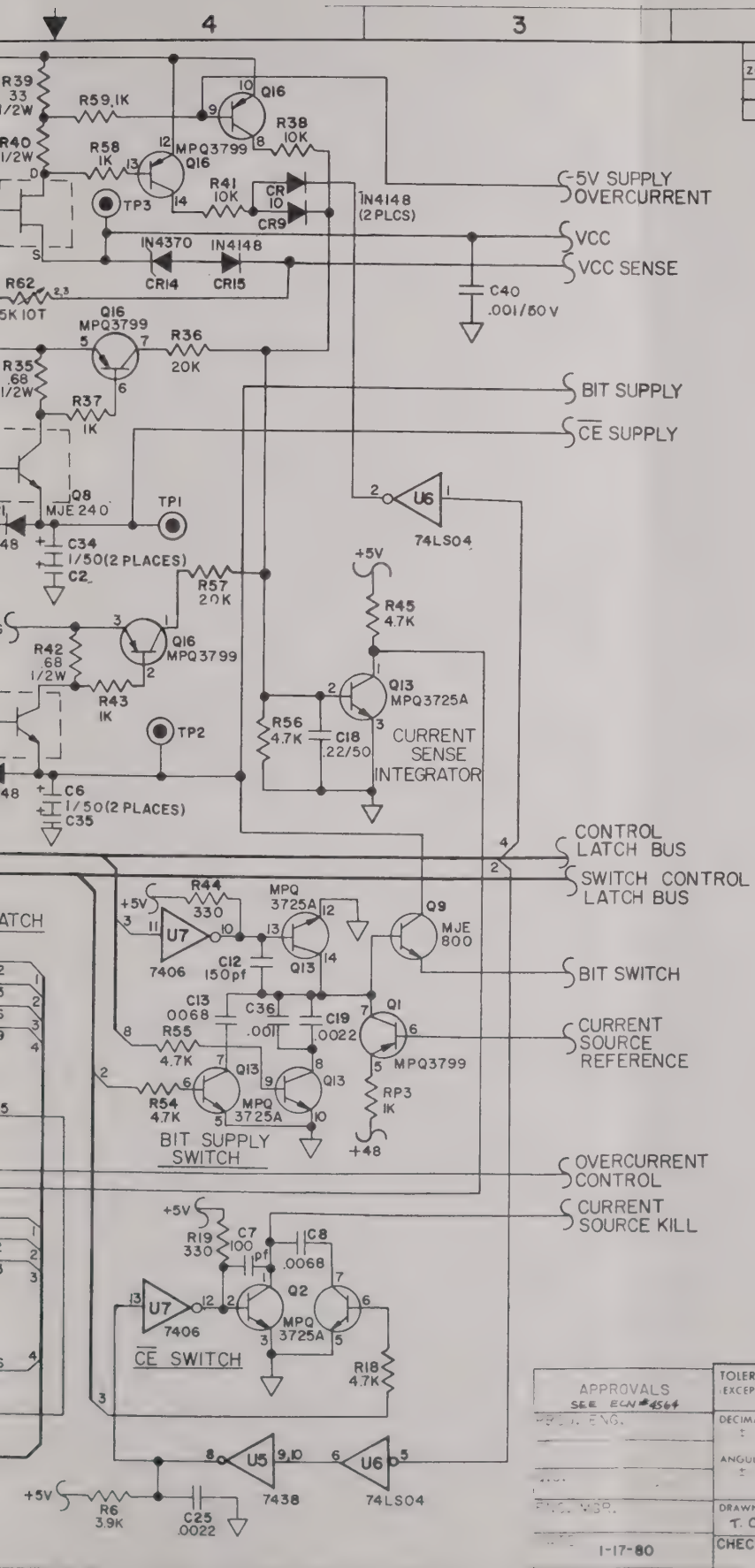

4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
C SEE SHEET ONE 1-17-
DATA SWITCHES
21 VREF
RP7
J1
U16 220 RP6 330 C10 250pf Q9 MJE251 40 PD1
U16 220 RP6 330 C6 250pf Q5 MJE251 41 PD2
U17 220 RP6 330 C9 250pf Q8 MJE251 42 PD3
U17 220 RP6 330 C5 250pf Q4 MJE251 43 PD4
U17 220 RP6 330 C12 250pf Q11 MJE251 25 PD5
U17 220 RP6 330 C8 250pf Q7 MJE251 24 PD6
U16 220 R21 330 C11 250pf Q10 MJE251 23 PD7
U16 R17 220 RP6 330 C7 250pf Q6 MJE251 22 PD8
U16, U17, MPQ3725A
12 BIT SWITCH
BIT SW
LOAD CLAMPS
LOAD CLAMPS
+5V
R24 470
CR5 IN4733
U3 TID121
U6 TID121
U5 TID139
U4 TID 139
RP2 10K
RP1 2K
R13 10K
CR3 IN4148
R14 2K
CR4 IN4148
J1
TP3
SP 48
SP 47
TP2
LOW RANGE LOADS
HIGH RANGE LOADS
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
ANGULAR ±
DRAWN BY
APPROVED BY
DATA I/O ISSAQUAH WASH
TITLE SCHEMATIC DIAGRAM UniPak ADDRESS CARD
SIZE D
CODE IDENT NO
DRAWING NO 008-1998
SCALE NONE
SHEET 2 OF 2
D
C
B
A


8
7
6
5
D
C
B
A
A0
A5
A1
A6
A2
A7
A3
A8
A4
A9
A10
A11
A12
A13
A14
A15
DO1
DI1
DO2
DI2
DO3
DI3
DO4
DI4
DO5
DI5
DO6
DI6
DO7
DI7
DO8
DI8
VER A
VER B
START
CLK INHIBIT
W/L
"26"
J1
J2, J3
P1
J1



APPROVALS	TOLERANCES (EXCEPT AS NOTED)	DATA I/O
PROJ. ENG.	DECIMAL	TITLE SCHEMATIC DIAGRAM UniPak MOTHERBOARD
PROD. ENG.	ANGULAR ±	
CONF. MANG.		
ENG. MGR.	DRAWN BY G. RYDER	SIZE D · CODE IDENT NO · DRAWING NO 008-1999
DATE 1-17-80	CHECK	SCALE NA · SHEET 1 OF 1


8
7
6
5
P1
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
A0
A1
A2
A3
C1
C5
C6
V·Ø2
+48V
RAW +18V
+PROG
-9V
+24V
+5V
GND
RP1, 3.3K
RP2, 3.3K
DATA LATCH
U12
74LS373
VCC SUPPLY DAC
U11
AD7524
5VREF
CE SUPPLY DAC
U10
AD7524
BIT SUPPLY DAC
U9
AD7524
5V REF
U4
LM148
VCC SUPPLY
U8
741
CE SUPPL
U1
BIT SUPPLY
U3
R66
4.99K
1%
R65
4.99K
1%
R64
4.99K
1%
R63
12.1K 1%
R15
32.4K,1%
R16
5K 10T
R34
32.4K,1%
R33
5K 10T
C22
.01/50
C38
27pf
C39
27pf
C33
0068
U6
74LS04
U14
74LS259
U13
74LS259
CONTROL LATCH
SWITCH CONTROL LATCH
ADDRES
DECODE



REVISIONS						
ZONE	LTR	DESCRIPTION	DR	CK	PE, APP	DATE
	A	RELEASE PER ECN 4564				5/82
	B	ECN #5045	SH			7/84

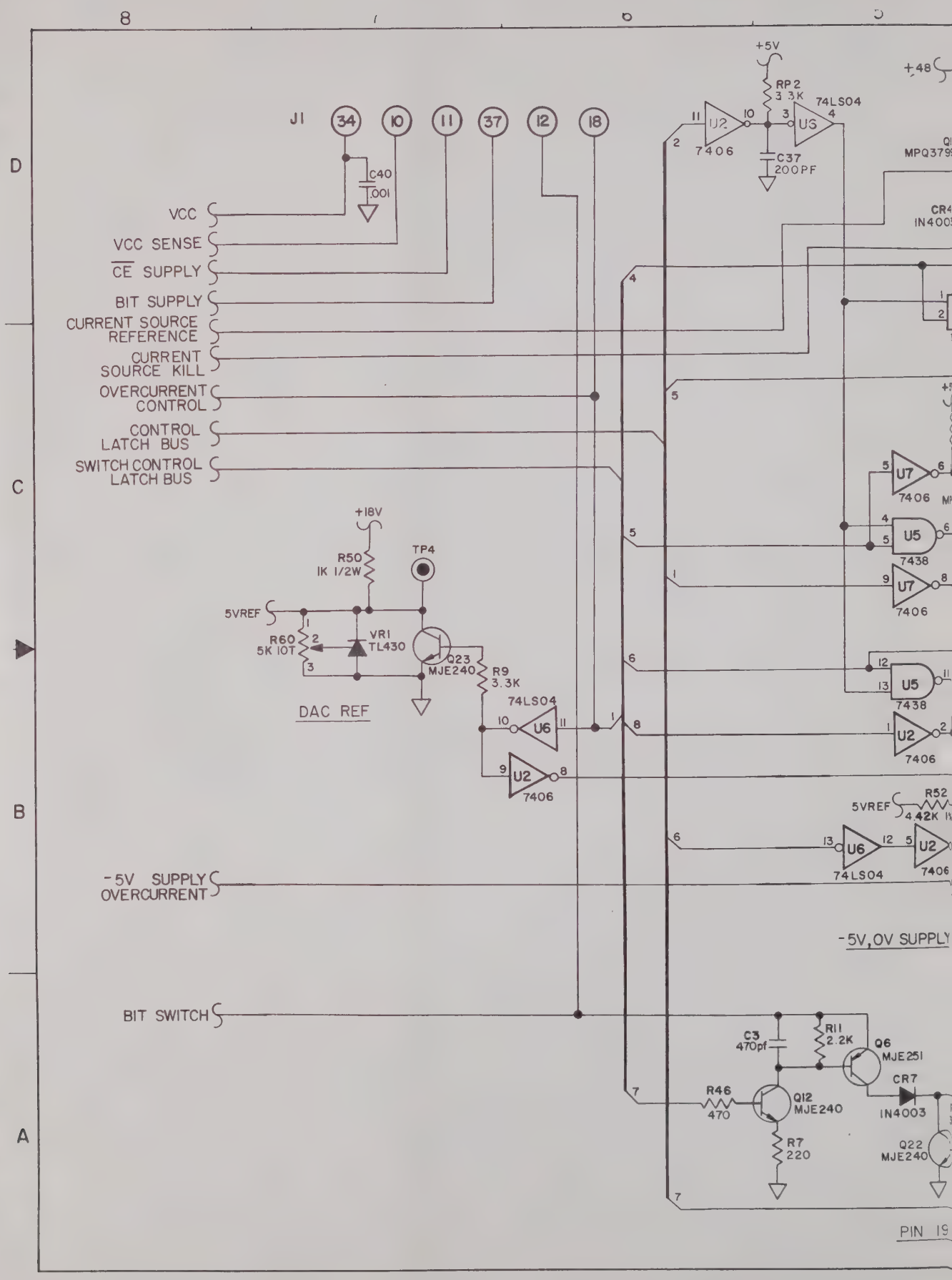
NOTES:

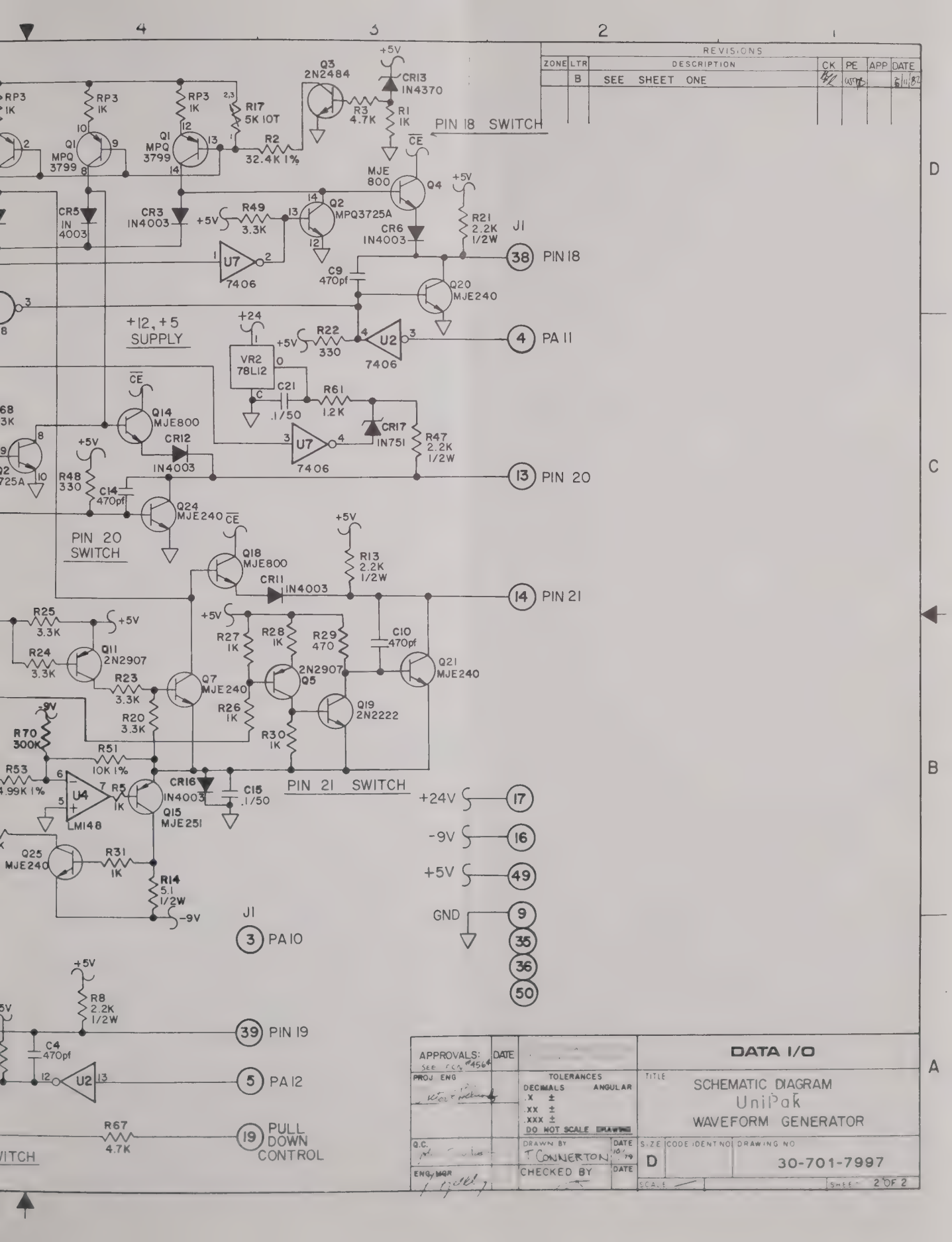
UNLESS OTHERWISE NOTED:

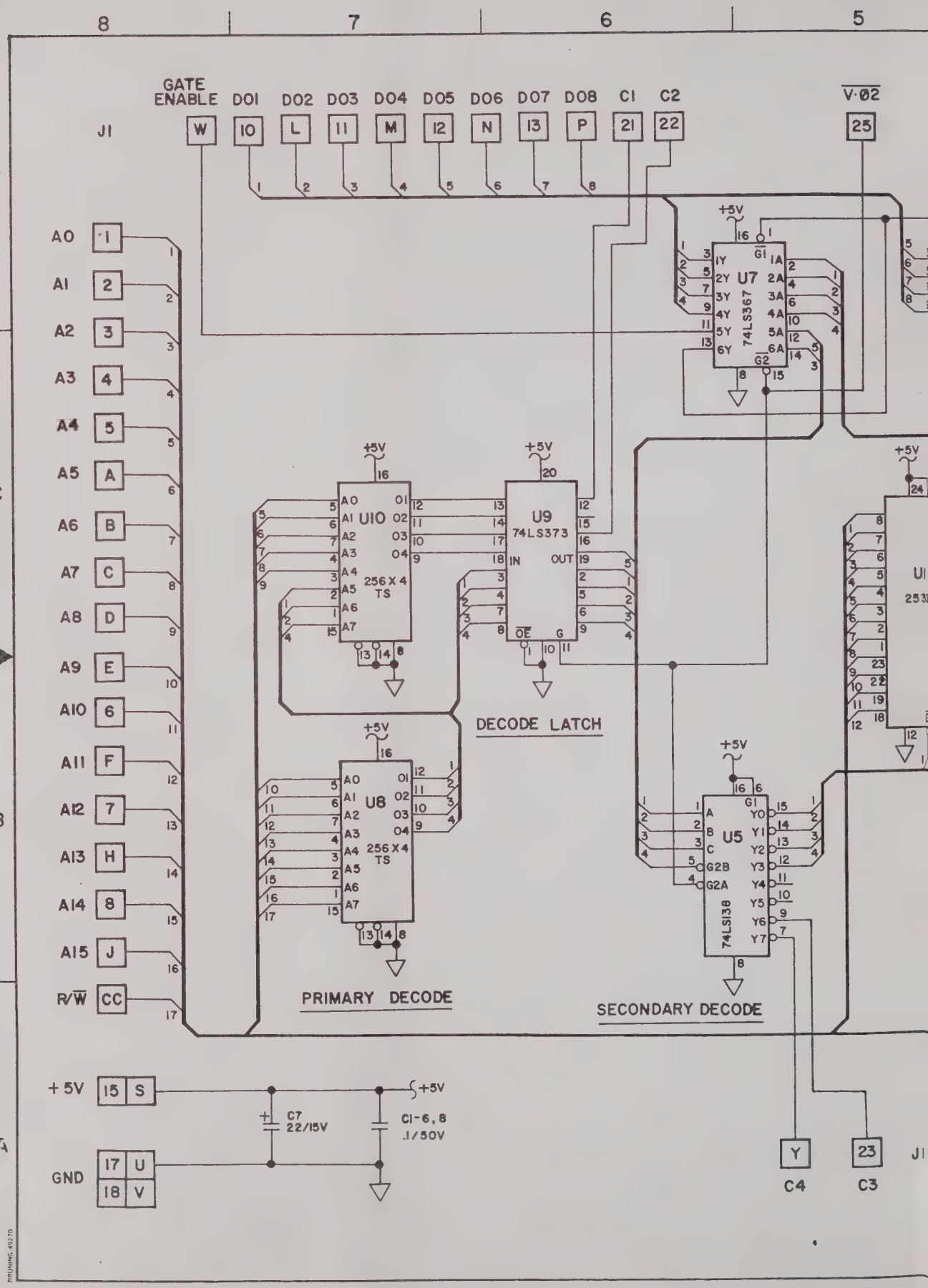
1. RESISTORS ARE 1/4W AND IN OHMS.
2. CAPACITORS ARE IN MICROFARADS.
3. U2, U5, U6, U7 - PIN 7 = GND, PIN 14 = +5V
   U12, U16 - PINS 18 & 10 = GND, PIN 20 = +5V
   U13, U14, U15 - PIN 8 = GND, 16 = +5V
   U4 PIN 4 = +24, PIN 11 = -9
4. LAST REF. DES. USED:
   RP3
   C40
   Q25
   U16
   CR17
   R70
   TP4
   VR2

P/N 701-7997-002

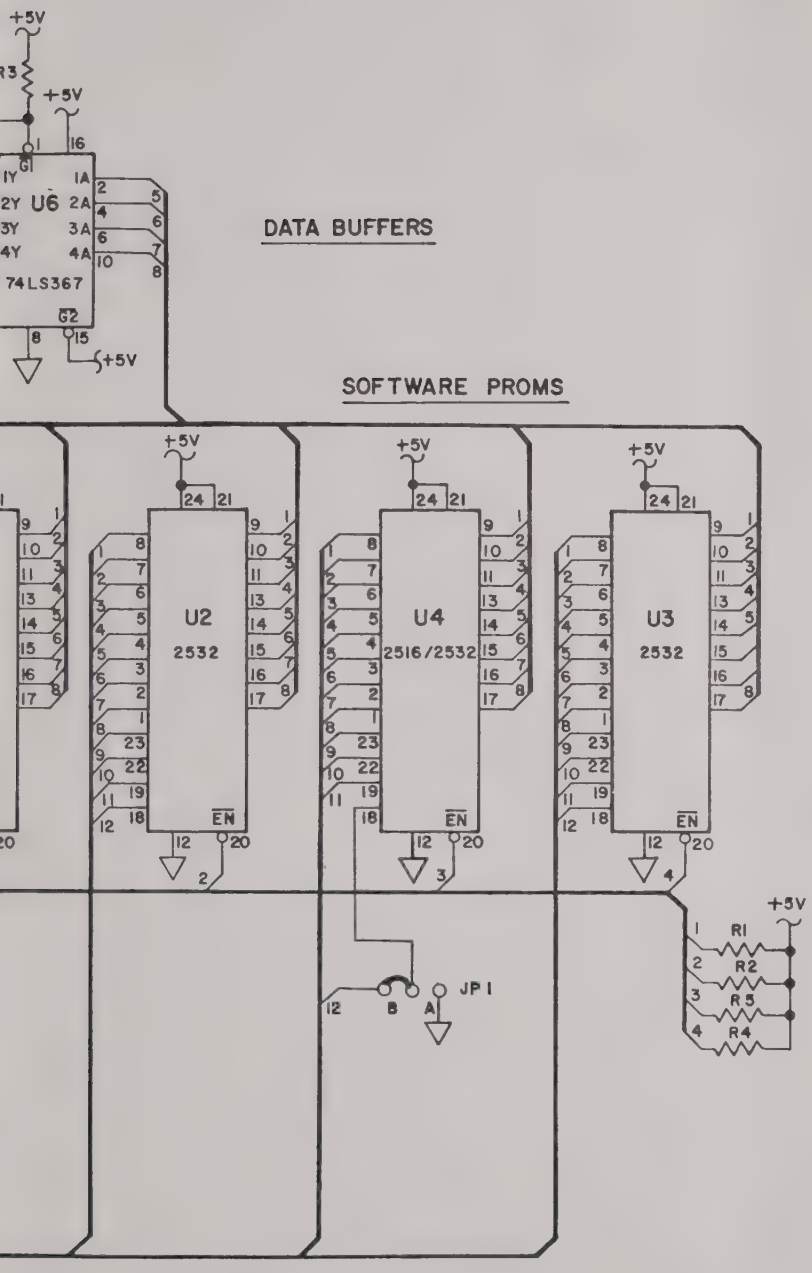
APPROVALS SEE ECN #4564	TOLERANCES (EXCEPT AS NOTED)	DATA I/O
DSGN. ENG.	DECIMAL ±	TITLE SCHEMATIC DIAGRAM UniPak WAVEFORM GENERATOR
	ANGULAR ±	
ENG. MGR.	DRAWN BY T. CONNERTON	SIZE D; CODE IDENT NO; DRAWING NO 30-701-7997
1-17-80	CHECKED BY	SCALE — SHEET 1 OF 2


J1
34
10
11
37
12
18
C40
.001
VCC
VCC SENSE
CE SUPPLY
BIT SUPPLY
CURRENT SOURCE REFERENCE
CURRENT SOURCE KILL
OVERCURRENT CONTROL
CONTROL LATCH BUS
SWITCH CONTROL LATCH BUS
+5V
RP2 3.3K
74LS04
U2
U3
7406
C37 200PF
+18V
R50 1K 1/2W
TP4
5VREF
R60 5K 10T
VR1 TL430
Q23 MJE240
R9 3.3K
DAC REF
74LS04
U6
U2
7406
U7
7406
U5
7438
U7
7406
U5
7438
U2
7406
5VREF
R52 4.42K
U6
74LS04
U2
7406
-5V SUPPLY OVERCURRENT
-5V,0V SUPPLY
BIT SWITCH
C3 470pf
R11 2.2K
Q6 MJE251
CR7 IN4003
R46 470
Q12 MJE240
R7 220
Q22 MJE240
PIN 19


REVISIONS
ZONE LTR DESCRIPTION CK PE APP DATE
B SEE SHEET ONE 5/4/82
PIN 18 SWITCH
+12, +5 SUPPLY
PIN 20 SWITCH
PIN 21 SWITCH
Q1 MPQ 3799
Q2 MPQ3725A
Q3 2N2484
Q4 MJE 800
Q5 2N2907
Q7 MJE240
Q11 2N2907
Q14 MJE800
Q15 MJE251
Q18 MJE800
Q19 2N2222
Q20 MJE240
Q21 MJE240
Q24 MJE240
Q25 MJE240
U2 7406
U4 LM148
U7 7406
VR2 78L12
CR1 IN4370
CR3 IN4003
CR5 IN 4003
CR6 IN4003
CR11 IN4003
CR12 IN4003
CR16 IN4003
CR17 IN751
R1 1K
R2 32.4K 1%
R3 4.7K
R4 1K
R5 1K
R8 2.2K 1/2W
R13 2.2K 1/2W
R14 5.1 1/2W
R17 5K 10T
R20 3.3K
R21 2.2K 1/2W
R22 330
R23 3.3K
R24 3.3K
R25 3.3K
R26 1K
R27 1K
R28 1K
R29 470
R30 1K
R31 1K
R47 2.2K 1/2W
R48 330
R49 3.3K
R51 10K 1%
R53 4.99K 1%
R61 1.2K
R67 4.7K
R70 300K
C4 470pf
C9 470pf
C10 470pf
C14 470pf
C15 .1/50
C21 .1/50
J1
38 PIN 18
4 PA 11
13 PIN 20
14 PIN 21
+24V 17
-9V 16
+5V 49
GND 9
35
36
50
3 PA 10
39 PIN 19
5 PA 12
19 PULL DOWN CONTROL
APPROVALS: DATE
SEE ECO #4564
PROJ ENG
Q.C.
ENG MGR
TOLERANCES
DECIMALS ANGULAR
.X ±
.XX ±
.XXX ±
DO NOT SCALE DRAWING
DRAWN BY T CONNERTON 10/19
CHECKED BY
DATA I/O
TITLE
SCHEMATIC DIAGRAM
UniPak
WAVEFORM GENERATOR
SIZE D
CODE IDENT NO
DRAWING NO 30-701-7997
SCALE
SHEET 2 OF 2


8
7
6
5
GATE ENABLE
D01
D02
D03
D04
D05
D06
D07
D08
C1
C2
V·02
J1
W
10
L
11
M
12
N
13
P
21
22
25
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
R/W
1
2
3
4
5
A
B
C
D
E
6
7
F
8
H
J
CC
U7
74LS367
U10
256 X 4
TS
U9
74LS373
U8
U5
74LS138
+5V
DECODE LATCH
PRIMARY DECODE
SECONDARY DECODE
+5V
GND
15
S
17
U
18
V
C7
22/15V
C1-6, 8
.1/50V
Y
C4
23
C3
J1

REVISIONS					
LTR	DESCRIPTION	DR	CHK	APPR'D	DATE
A	RELEASE	TC			5-4-81
B	E.F.	GR1			7/

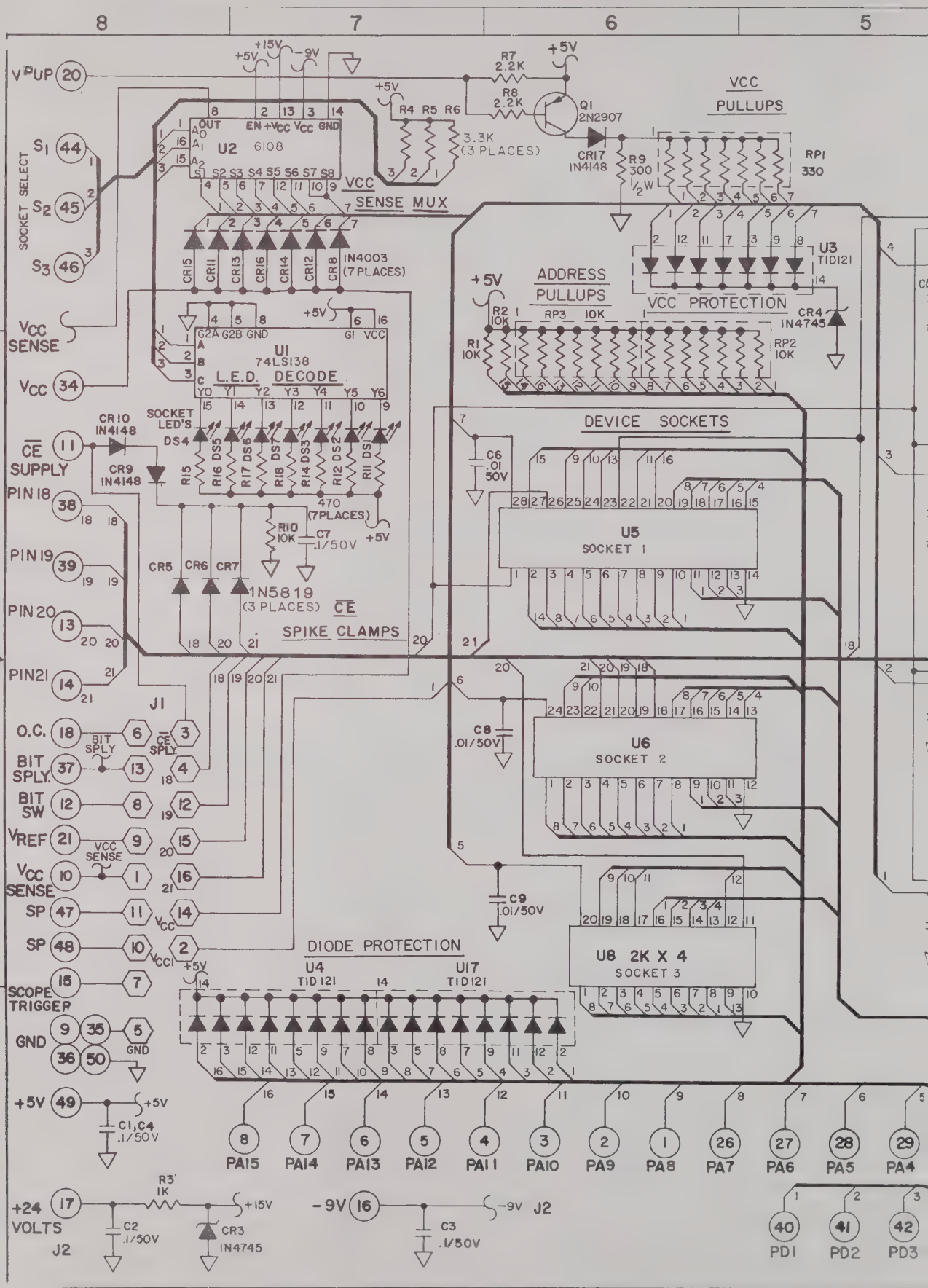


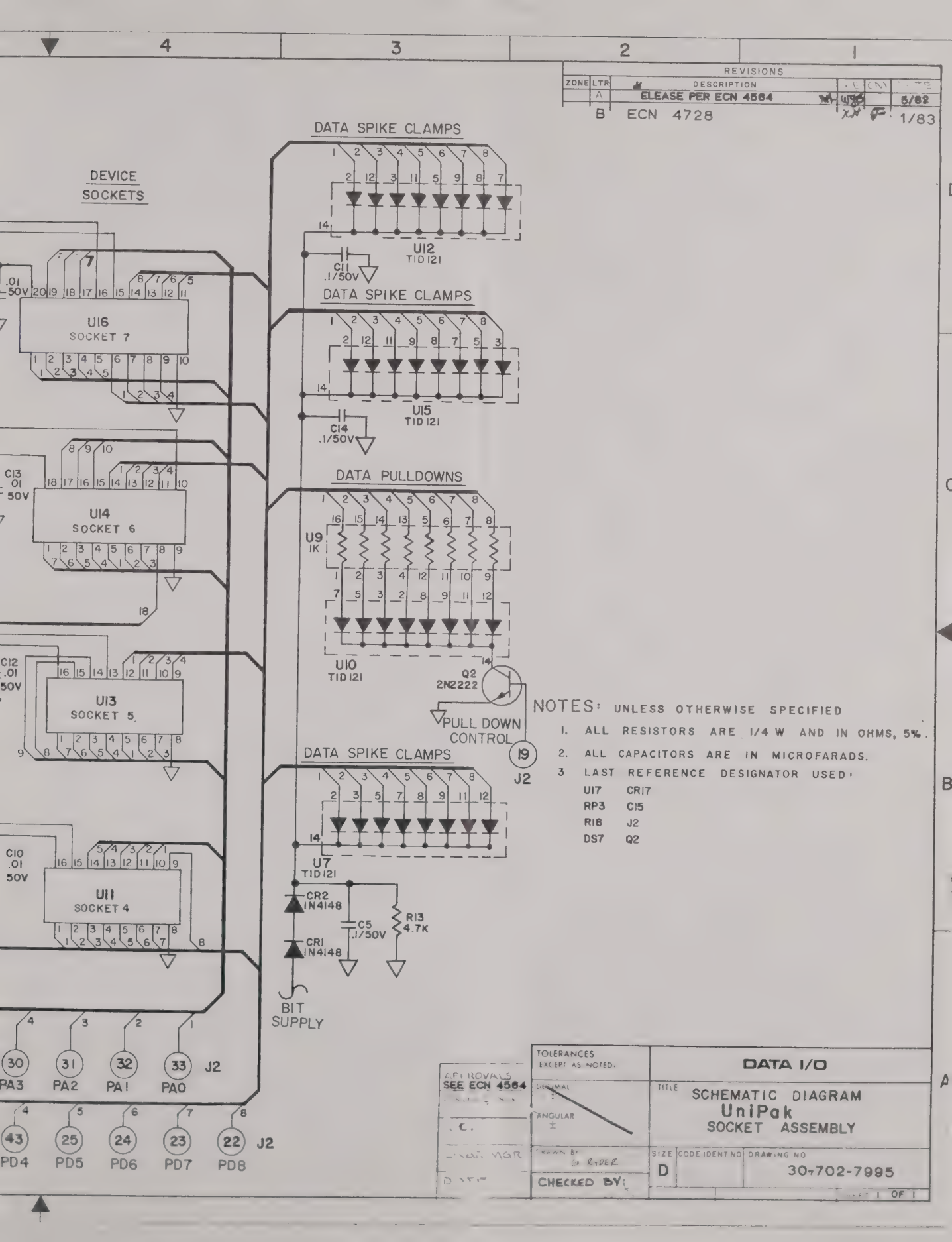
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 3.3K OHMS 1/4W 5%
2. ALL CAPACITORS ARE IN MICROFARADS.
3. JP 1, POS. B
4. LAST REFERENCE DESIGNATOR USED:
   - C8
   - R5
   - U10
   - JP 1

P/N 702-0045-002

APPROVALS:		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		DATA I/O	
DSN ENGR: Henry M. Kelly	DATE: 5/5/81	TOLERANCES, UNLESS OTHERWISE SPECIFIED: XX ±, XXX ±, ANGULAR		TITLE: SCHEMATIC DIAGRAM UNIPAK MEMORY	
MFG ENGR: M. J. Wiseman	DATE: 5-5-81				
QUAL ASSUR.	DATE: 5-5-81	DRAWN BY: TCC	DATE: 3-16-81	SIZE: D	CODE INDENT. NO.: 54193
ENGR MGR: Peter H. Dile	DATE: 5-5-81	CHECKED BY: Thomas H. Hill	DATE: 5-4-81	DRAWING NO.: 30-702-0045	
				SCALE: NONE	SHEET: 1 OF 1


8
7
6
5
D
C
B
A
VPUP 20
+15V
-9V
+5V
R7 2.2K
R8 2.2K
Q1 2N2907
VCC PULLUPS
R4 R5 R6
3.3K (3 PLACES)
CR17 IN4148
R9 300 1/2W
RP1 330
S1 44
S2 45
S3 46
SOCKET SELECT
U2 6108
OUT EN +VCC VCC GND
A0 A1 A2
S1 S2 S3 S4 S5 S6 S7 S8
VCC SENSE MUX
CR15 CR11 CR13 CR16 CR14 CR12 CR8
IN4003 (7 PLACES)
U3 TID121
VCC PROTECTION
CR4 IN4745
ADDRESS PULLUPS
R2 10K
RP3 10K
R1 10K
RP2 10K
VCC SENSE
VCC 34
U1 74LS138
L.E.D. DECODE
G2A G2B GND G1 VCC
Y0 Y1 Y2 Y3 Y4 Y5 Y6
SOCKET LED'S
DS4
R15 R16 DS5 R17 DS6 R18 DS7 R14 DS3 R12 DS2 R11 DS1
470 (7PLACES)
CR10 IN4148
CR9 IN4148
CE SUPPLY 11
PIN 18 38
PIN 19 39
PIN 20 13
PIN 21 14
R10 10K
C7 .1/50V
CR5 CR6 CR7
1N5819 (3 PLACES) CE
SPIKE CLAMPS
DEVICE SOCKETS
C6 .01 50V
U5 SOCKET 1
C8 .01/50V
U6 SOCKET 2
C9 .01/50V
U8 2K X 4 SOCKET 3
J1
O.C. 18
BIT SPLY. 37
BIT SW 12
VREF 21
VCC SENSE 10
SP 47
SP 48
SCOPE TRIGGER 15
GND 9 35 36 50
DIODE PROTECTION
U4 TID121
U17 TID121
+5V 49
C1, C4 .1/50V
PA15 PA14 PA13 PA12 PA11 PA10 PA9 PA8 PA7 PA6 PA5 PA4
+24 VOLTS 17
R3 1K
C2 .1/50V
CR3 IN4745
J2
-9V 16
C3 .1/50V
PD1 PD2 PD3


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION
A RELEASE PER ECN 4564 5/82
B ECN 4728 1/83
DEVICE SOCKETS
DATA SPIKE CLAMPS
U12 TID121
C11 .1/50V
DATA SPIKE CLAMPS
U15 TID121
C14 .1/50V
DATA PULLDOWNS
U9 1K
U10 TID121
Q2 2N2222
PULL DOWN CONTROL
19 J2
DATA SPIKE CLAMPS
U7 TID121
CR2 IN4148
CR1 IN4148
C5 .1/50V
R13 4.7K
BIT SUPPLY
U16 SOCKET 7
U14 SOCKET 6
U13 SOCKET 5
U11 SOCKET 4
C13 .01 50V
C12 .01 50V
C10 .01 50V
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W AND IN OHMS, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3 LAST REFERENCE DESIGNATOR USED:
UI7 CRI7
RP3 C15
RI8 J2
DS7 Q2
30 PA3
31 PA2
32 PA1
33 PA0
J2
43 PD4
25 PD5
24 PD6
23 PD7
22 PD8
J2
APPROVALS SEE ECN 4564
TOLERANCES EXCEPT AS NOTED:
DECIMAL
ANGULAR
DRAWN BY G. RYDER
CHECKED BY:
DATA I/O
TITLE SCHEMATIC DIAGRAM UniPak SOCKET ASSEMBLY
SIZE D
CODE IDENT NO
DRAWING NO 30-702-7995
SHEET 1 OF 1

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Direct Sales and Service Offices

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The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual? _____

How can this manual be improved? _____

_____

_____

Additional comments: _____

_____

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Company _____

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Did the packaging of this equipment exhibit any outward signs of physical damage? ☐ YES ☐ NO

Did this equipment arrive intact, without loose parts or cable damage? ☐ YES ☐ NO

Did the equipment operate on power-up? ☐ YES ☐ NO

Did you attain adequate system performance? ☐ YES ☐ NO

Were any electrical adjustments required? ☐ YES ☐ NO

If you required assistance, was a local Data I/O representative contacted? ☐ YES ☐ NO

Comments: _____

_____

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